

MODEL NAME :**VAW03**

PCB NO : **LA-9103P**

BOM P/N : **DA60000UT00 LA-9103P M/B**

DA40001FO00 LS-9101P POWER BUTTON/B

DA40001FP00 LS-9102P USB/B

DA40001FQ00 LS-9103P TP BUTTON/B

Inspiron Value OAK(Essentials) 15 UMA (Comal Richland)

Inspiron Value OAK(Essentials) 15 Discrete#1 (Comal Richland, AMD Mars Pro)

Inspiron MainStream OAK(Essentials) 15 UMA (Comal Richland)

Inspiron MainStream OAK(Essentials) 15 Discrete#2 (Comal Richland, AMD Mars Pro)

Vostro Value OAK(Essentials) 15 UMA (Comal Richland)

Dell / Compal Confidential

Schematic Document

AMD FP2 Richland Processor with DDRIII + Bolton M3 FCH

AMD VGA Sun XT

46@ : for 46 level

@ : Nopop Component

CONN@ : Connector Component

UMA@ : Only for UMA

DIS@ : Only for Discrete

GCLK@ : Green CLK implemented

NGCLK@ : Non Green CLK implemented

@3221: ALC 3221

@3223 : ALC 3223

EMC@ : EMC Parts

2nd@ : for APL3512 2nd source control

(RN9, RV32, RL22)

2012-11-26

Rev: 0.2

R1@ : R1 P/N for PCB

R3@ : R3 P/N for PCB

THR1@ : Thames-XT R1 P/N

THR3@ : Thames-XT R3 P/N

CHR1@ : Chelsea-Pro R1 P/N

CHR3@ : Chelsea-Pro R3 P/N

R@ : RTD2132-R

S@ : RTD2132-S

X76@ : VRAM Group

CH@ : Chelsea M2

SE@ : Seymour M2

TH@ : Thames-XT

Mars@ : Mars Pro M2

A4R1@ : A4 APU-R1

A6R1@ : A6 APU-R1

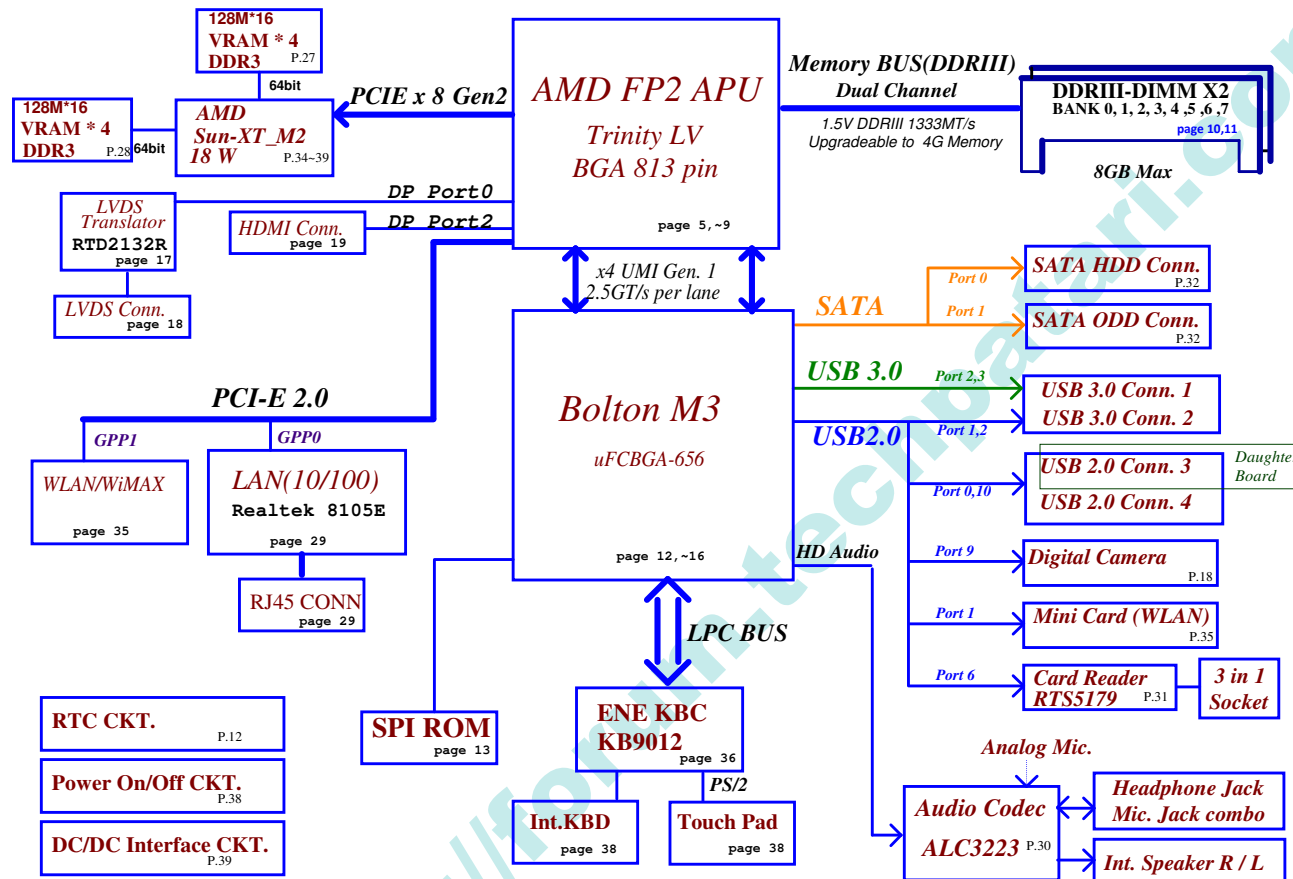
A8R1@ : A8 APU-R1

A8@ : A8 APU Symbol

Hud@ : HUDSON-M3

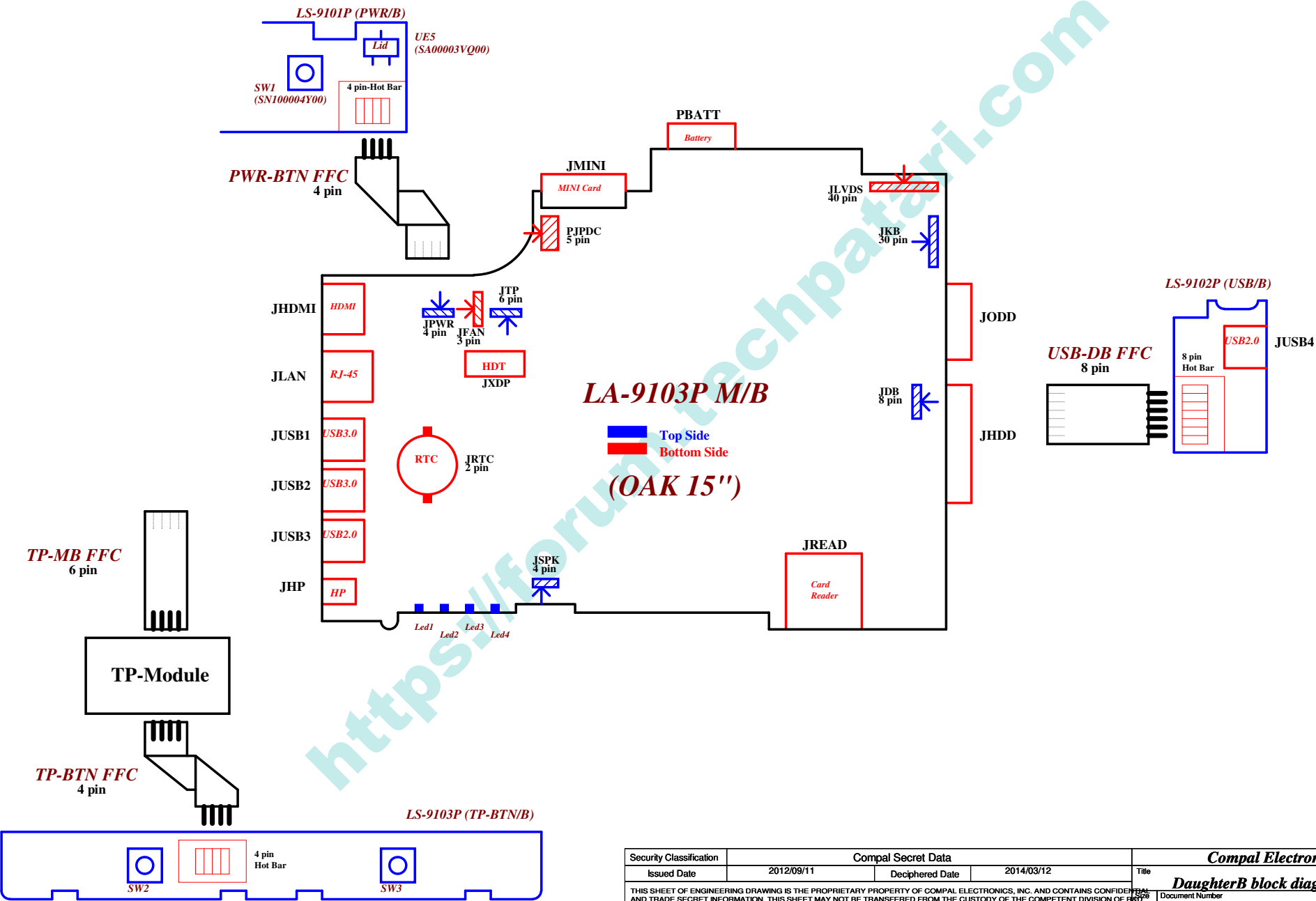
Bol@ : BOLTON-M3

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		Rev	0.1



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Project Code : VAW03
File Name : LA-9103P



Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

EC SM Bus1 address

EC SM Bus2 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	000 1011	11h 0x16	ADM1032ARMZ	100 1101	4Dh 0x9A
Charger IC	000 1001	09h 0x12	SB-TSI	100 1100	4Ch 0x98
			RTD2132	100 1010	4Ah 0x94
			GPU	100 0001	41h 0x82

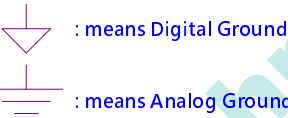
SM Bus Controller 0 (FCH_SMB1 ~ FCH_SMB4, SMB_ALERT#)

Device	Address	HEX
APU SIC/SID (FCH_SMB3)		

SM Bus Controller 1 (FCH_SMB0)

Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90
DDR DIMM2 (FCH_SMB0)	1001-001xb	92
WLAN (FCH_SMB0)		

Symbol Note :



FCH

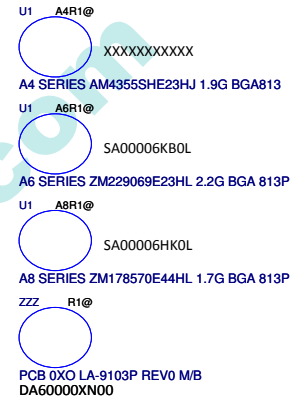
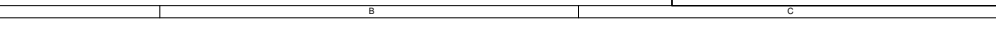
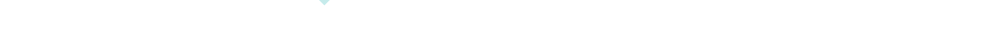
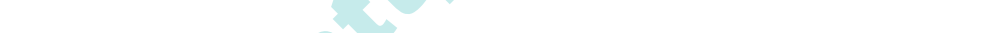
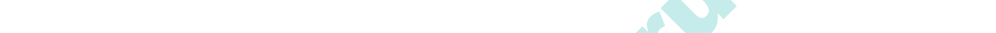
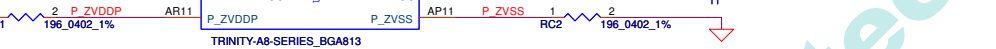
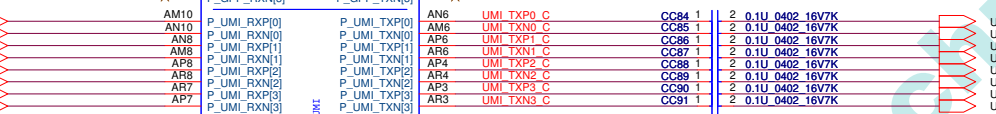
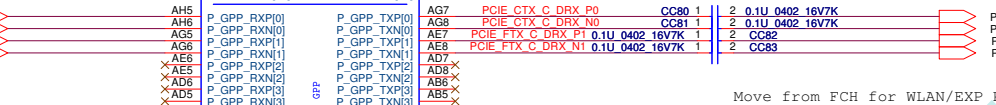
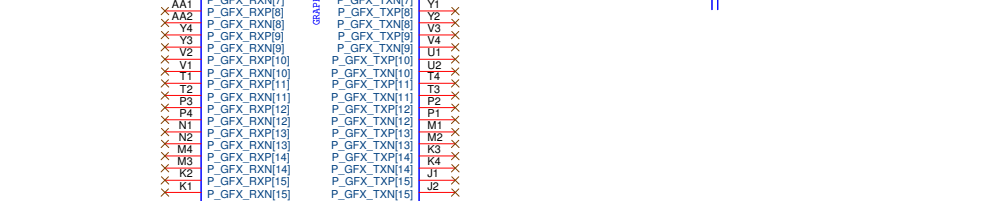
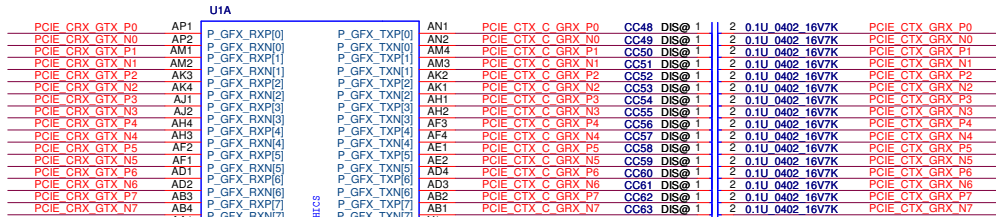
USB PORT#	DESTINATION
0	USB conn.3 DEBUG PORT
1	MINI CARD (WLAN)
2	USB conn.4
3	NC
4	NC
5	NC
6	Card Reader
7	NC
8	NC
9	Camera
10	USB conn.2
11	NC
12	NC
13	USB conn.1

CLK	DIFFERENTIAL	DESTINATION
	CLKOUT_PCIE0	None
	CLKOUT_PCIE1	None
	CLKOUT_PCIE2	10/100 LAN
	CLKOUT_PCIE3	MINI CARD WLAN
	CLKOUT_PCIE4	None
	CLKOUT_PCIE5	None
	CLKOUT_PCIE6	None
	CLKOUT_PCIE7	None
	CLKOUT_PEG_B	None

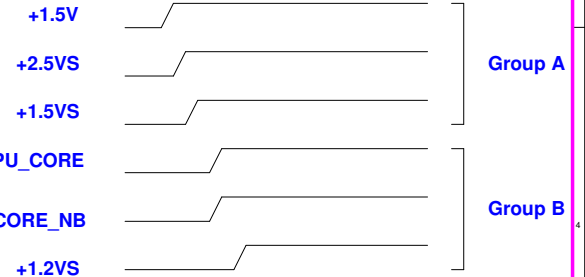
SATA	DESTINATION
SATA0	HDD
SATA1	ODD
SATA2	None
SATA3	None
SATA4	None
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	10/100 LAN
Lane 2	MINI CARD (WLAN)
Lane 3	None
Lane 4	None
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

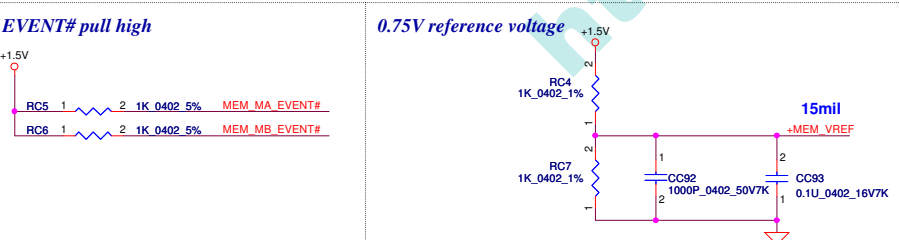
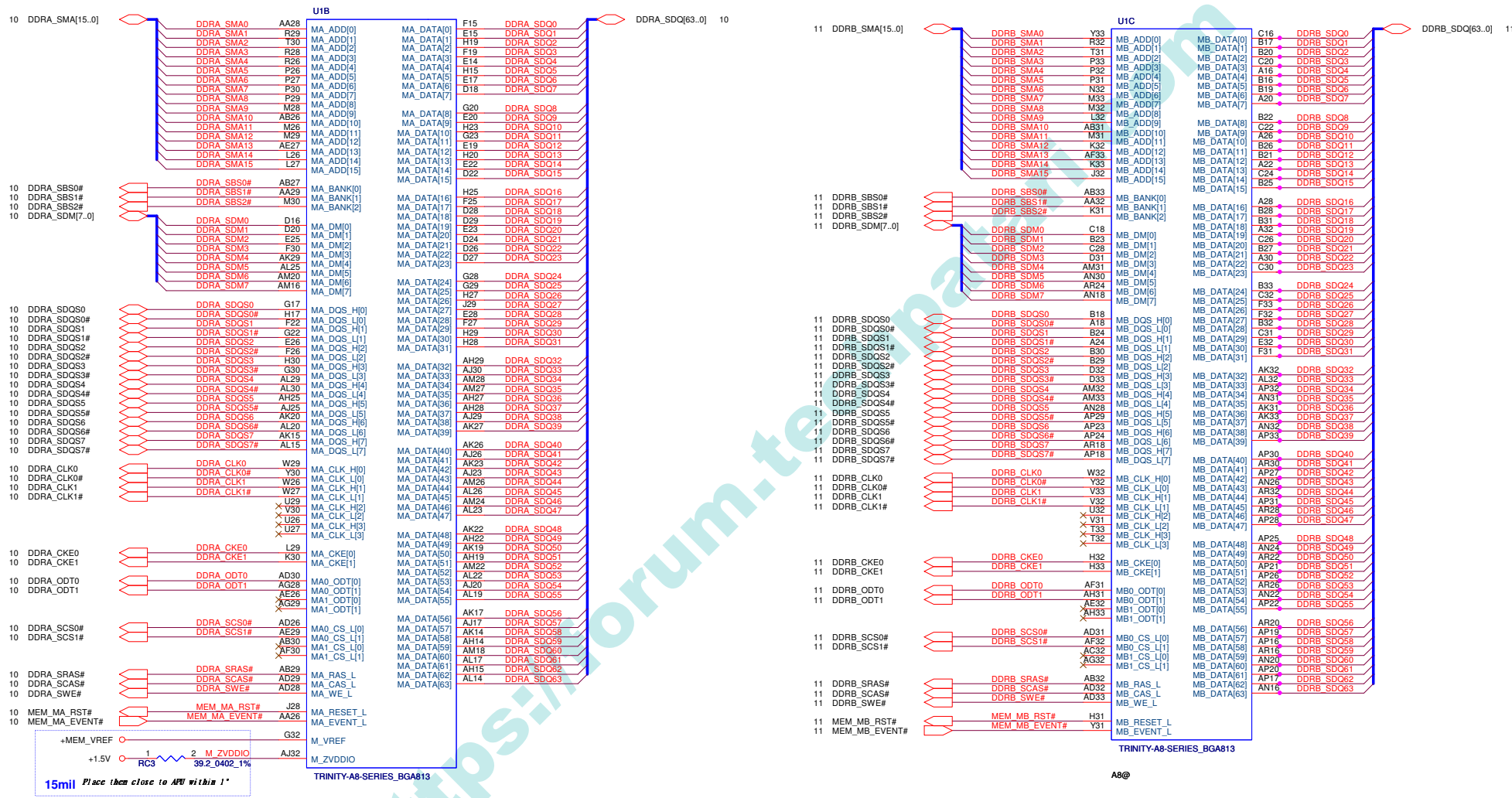
21 PCIE_CRX_GTX_P[0..7] 21 PCIE_CTX_GRX_P[0..7]
21 PCIE_CRX_GTX_N[0..7] 21 PCIE_CTX_GRX_N[0..7]



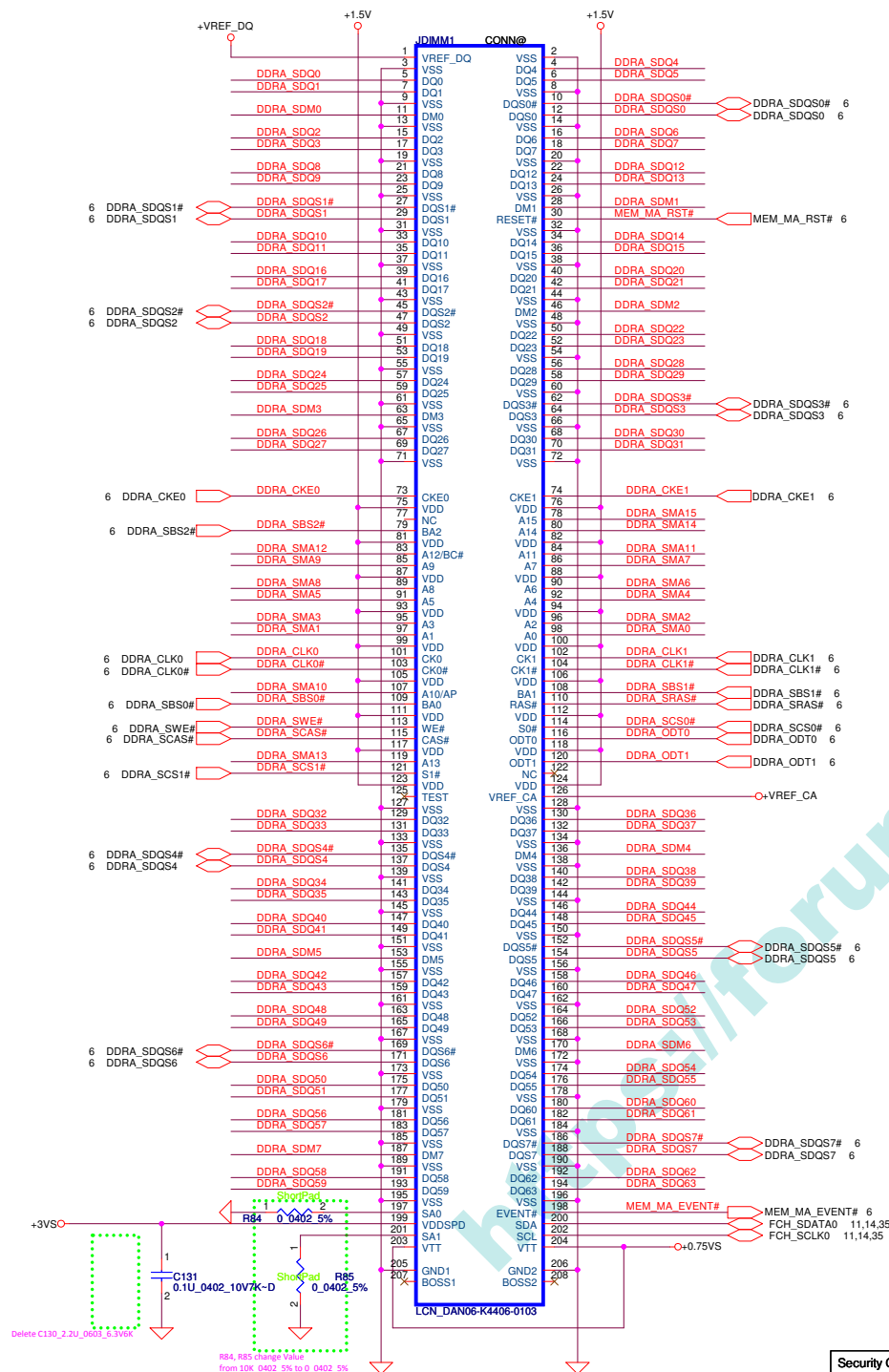
Power Sequence of APU



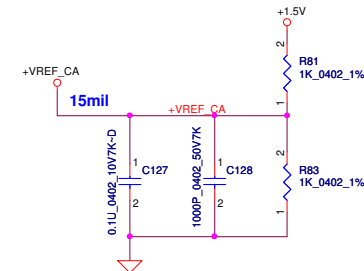
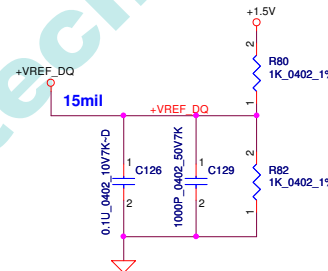
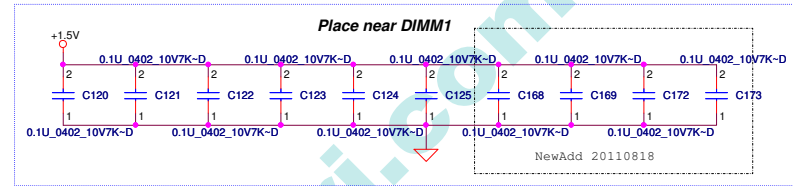
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
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Title				FP2 PCIE/UMI				Rev 0.1			
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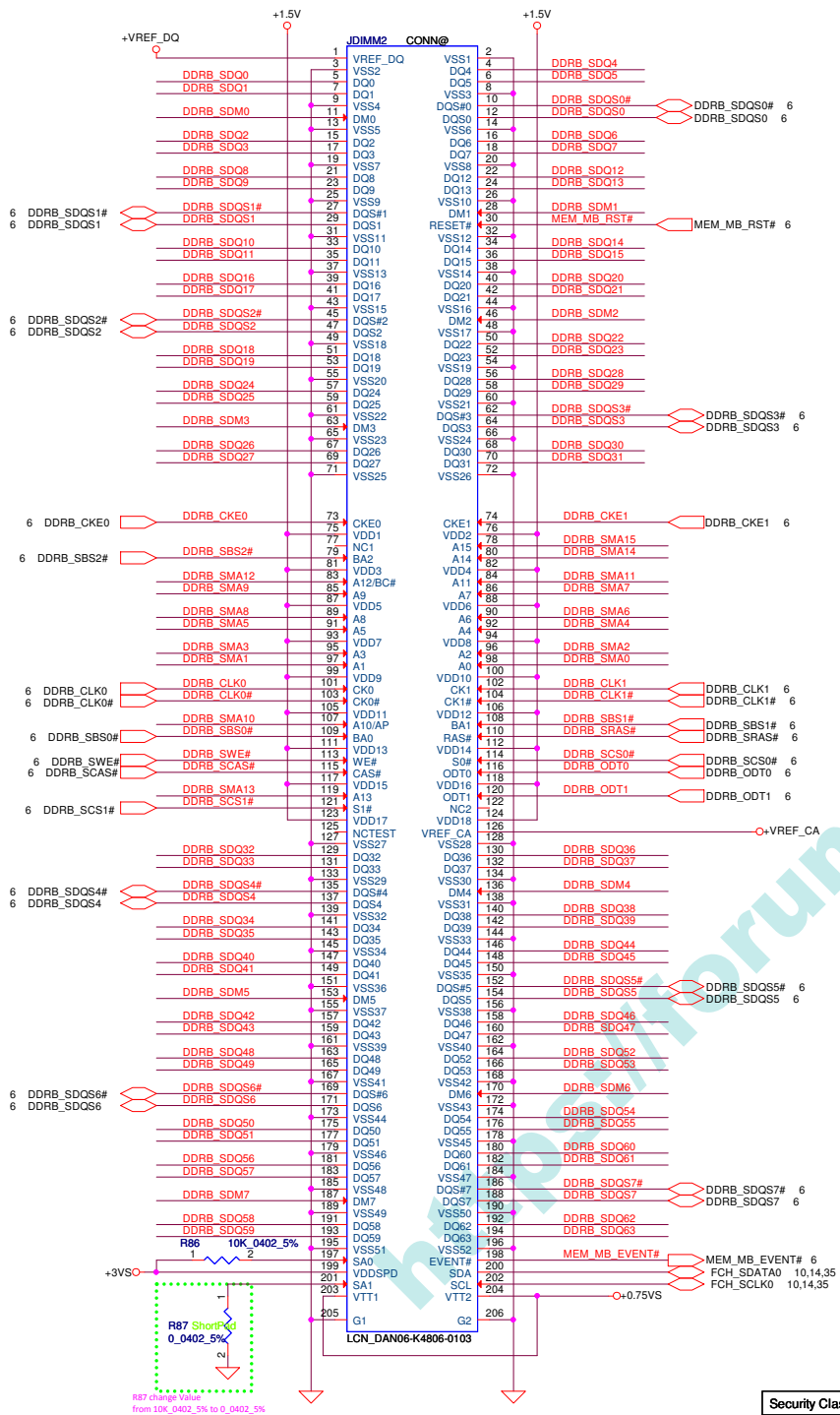
Security Classification		Compal Secret Data				Compal Electronics, Inc.					
Issued Date		2012/09/11		Deciphered Date		2014/03/12		Title			
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						Document Number		LA-9103P		Rev	
						Custom				0.1	
						Date:		Tuesday, November 27, 2012		Sheet 6 of 52	



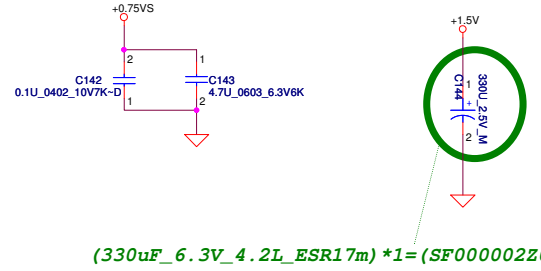
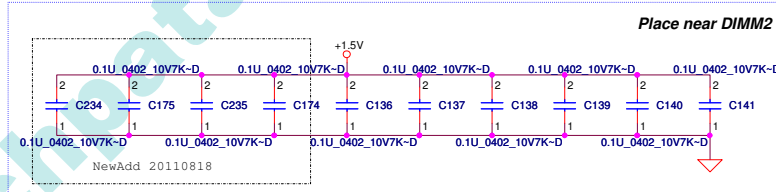
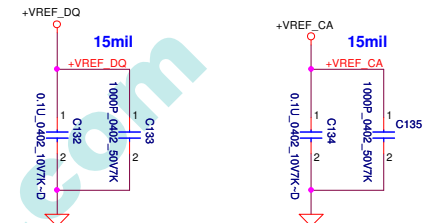
DDR_A_SDQ[0..63] 6
DDR_A_SDM[0..7] 6
DDR_A_SMA[0..15] 6



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				Document Number				LA-9103P			
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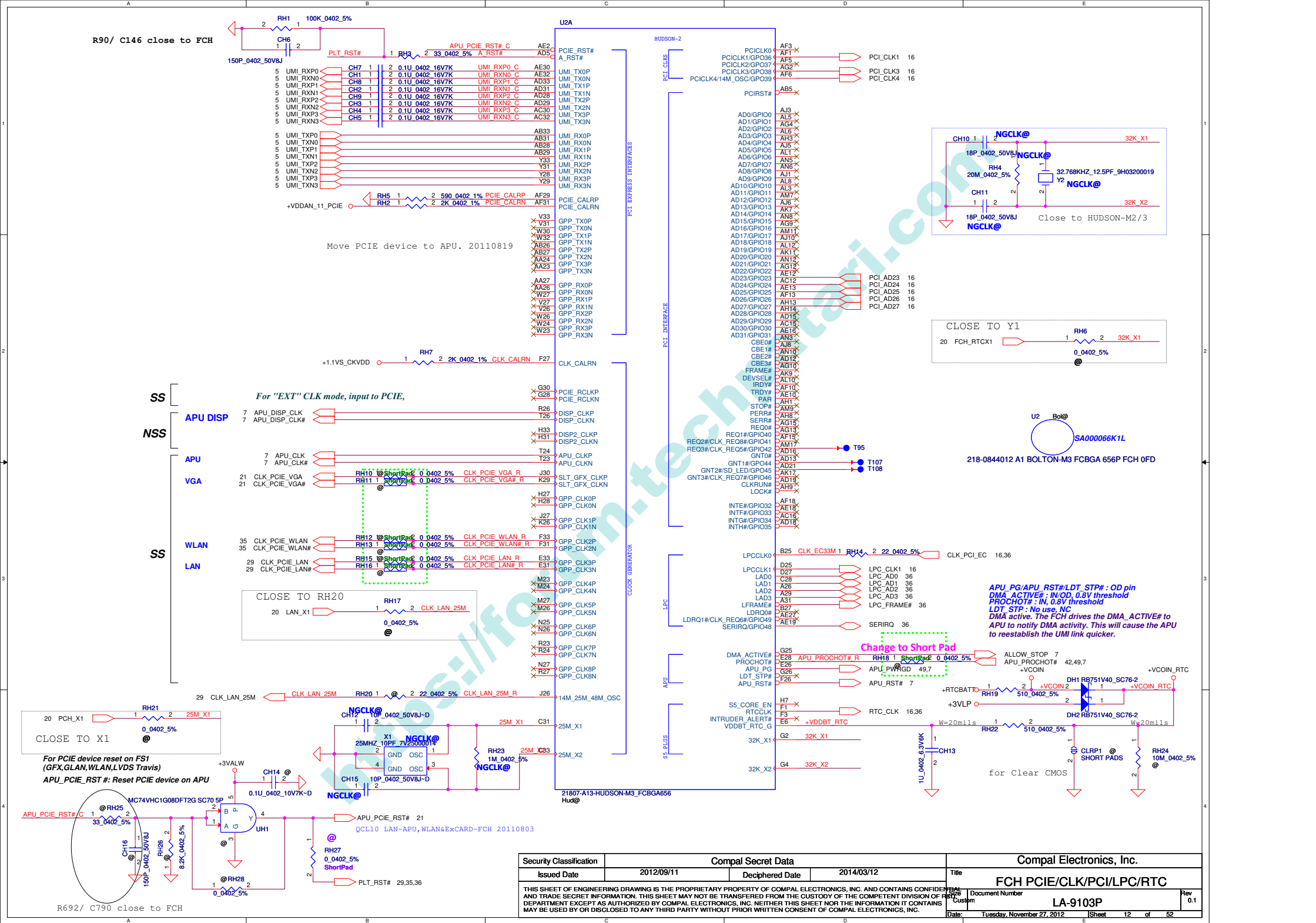
DDR_B_SDQ[0..63] 6
DDR_B_SDM[0..7] 6
DDR_B_SMA[0..15] 6



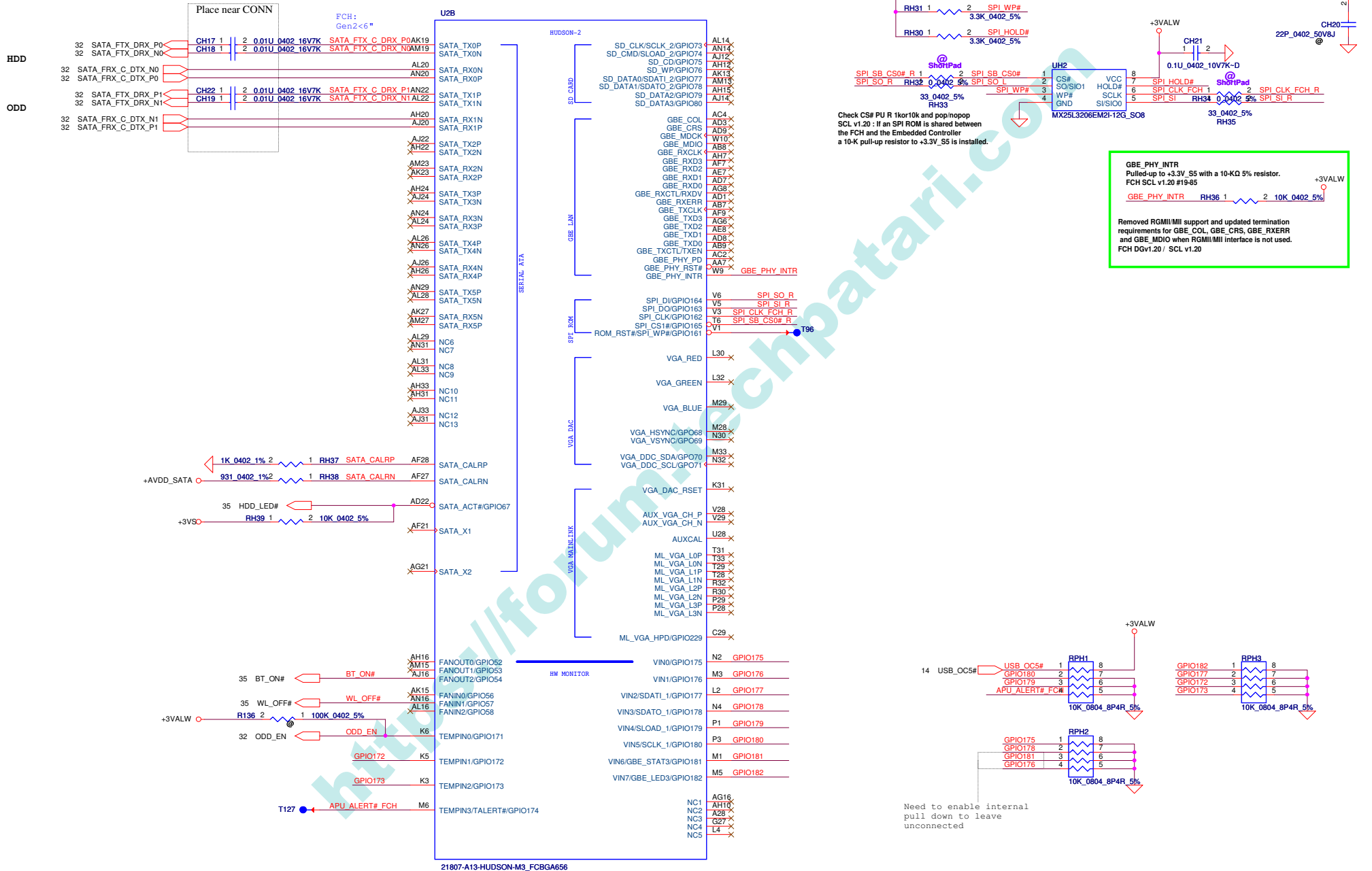
(330uF_6.3V_4.2L_ESR17m)*1=(SF000002Z00)

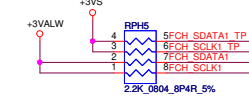
Reserve H:8mm
<Address: 01>

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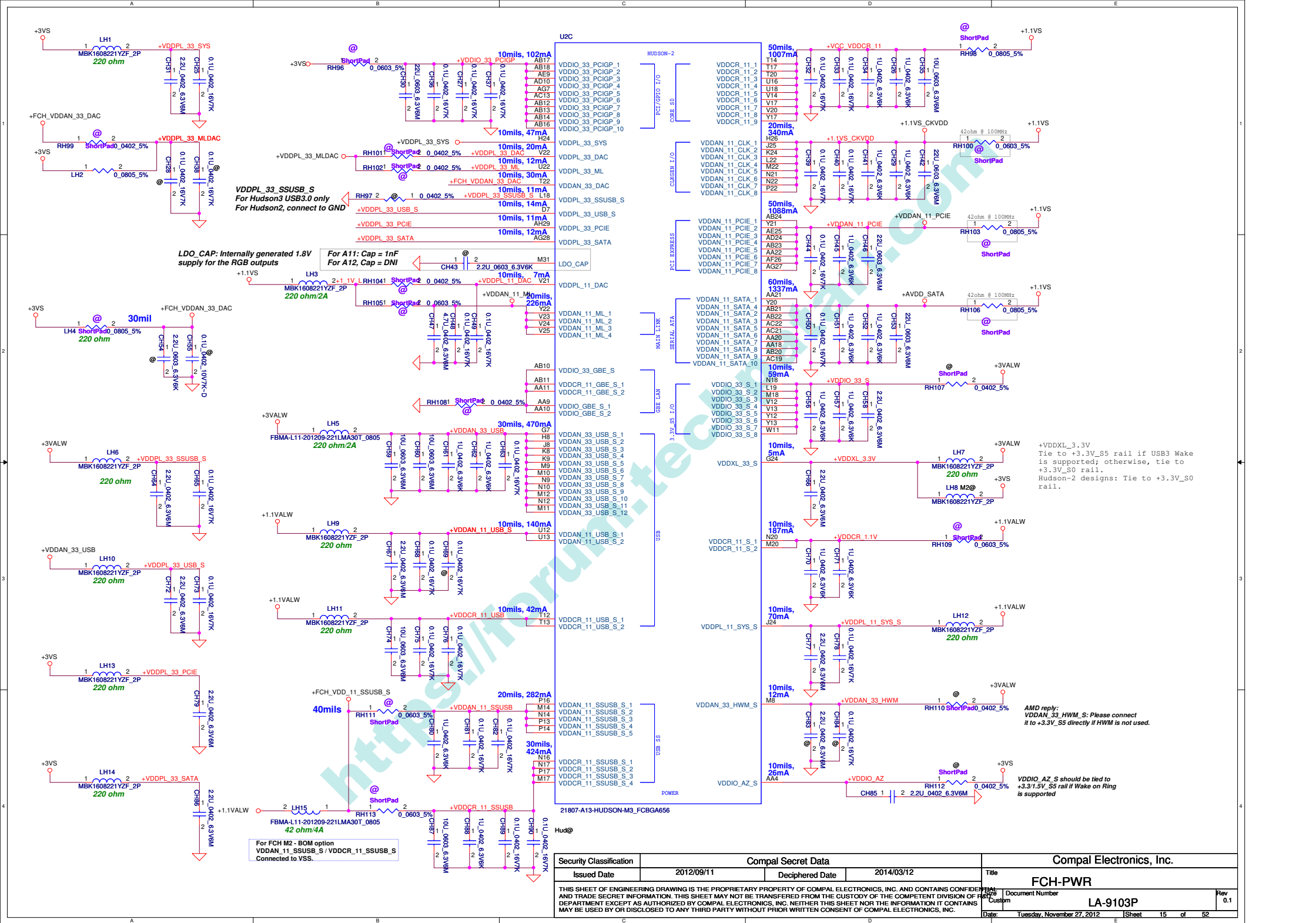


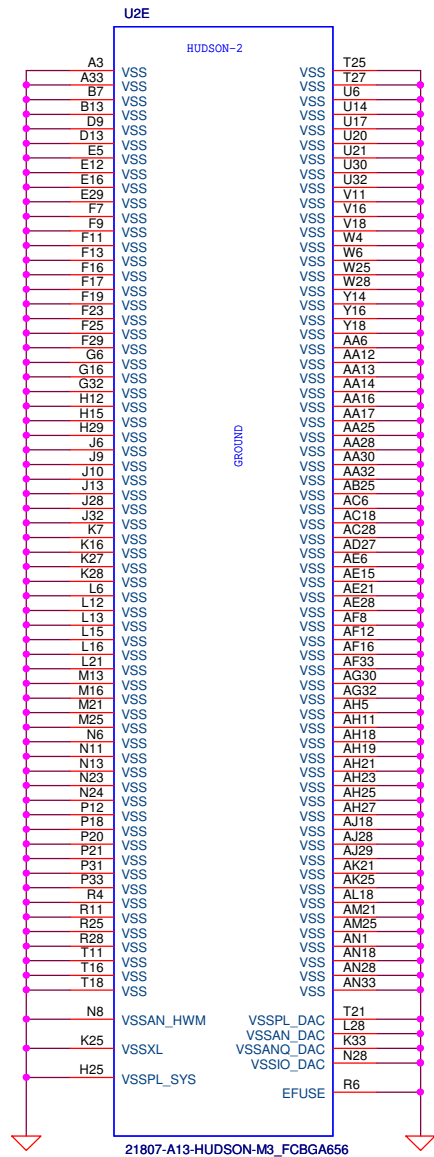
4MB SPI ROM & Non-share ROM.





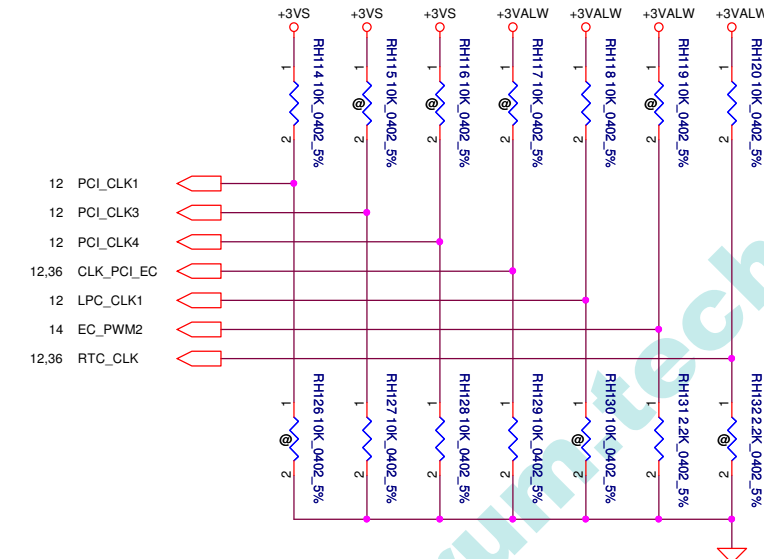
Issued Date	2/27/2013	Deciphered Date	2/27/2013	FCH-ACPI/USB/HDA/GPIO				
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STRAP PINS

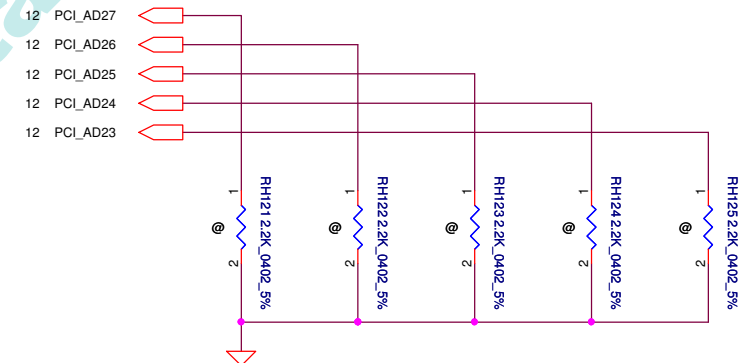
	PCI_CLK1	PCI_CLK3	PCI_CLK4	CLK_PCI_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED



DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

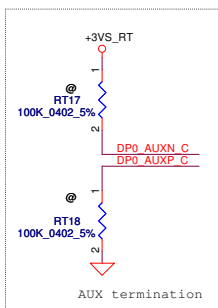
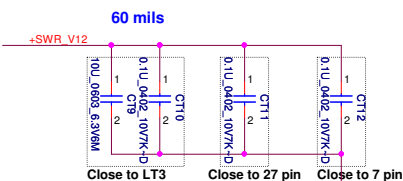
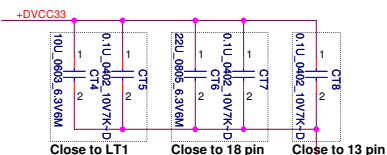
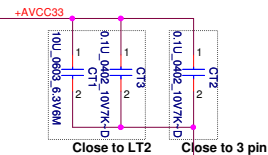
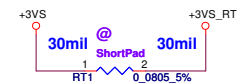
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



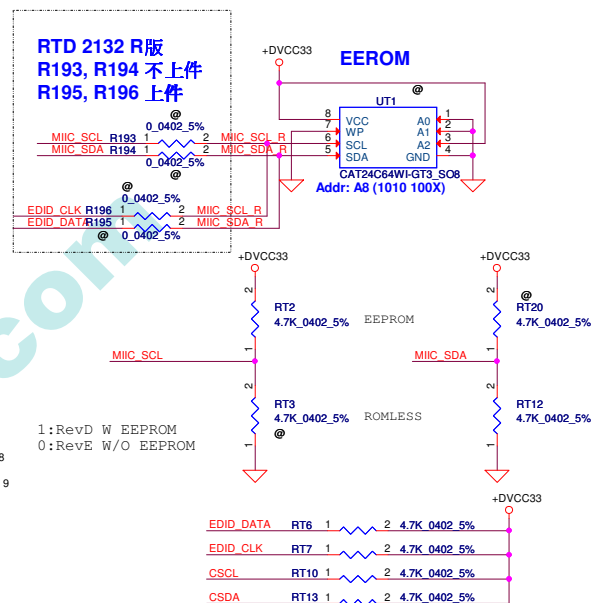
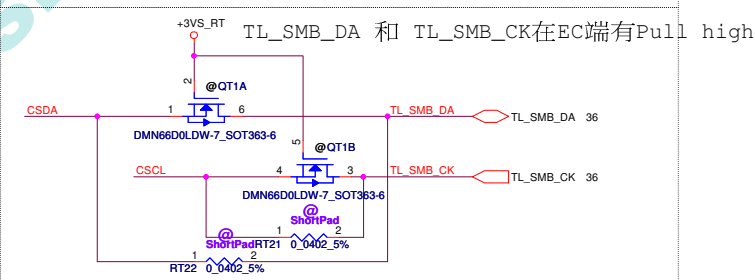
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Power Consumption:

Pin3 (DPV33) < 20mA
 Pin 7 (DP_V12) < 100mA
 Pin 11 (SWR_VCKK) < 100mA (layout trace > 60 mil)
 Pin 12 (SWR_LX) < 600mA (layout trace > 60 mil)
 Pin 13 (SWR_VDD) < 200mA (layout trace > 40 mil)
 Pin 18 (PVCC) < 50 mA
 Pin 27 (VCKK) < 50mA

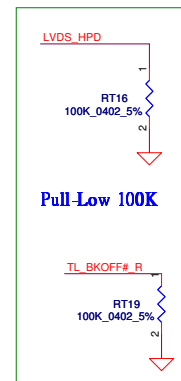


Vendor advise reserve it



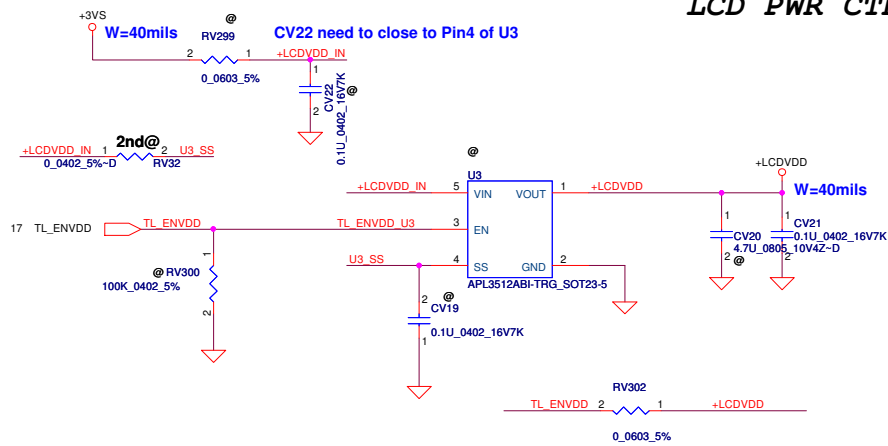
1:RevD W EEPROM
 0:RevE W/O EEPROM

		Pin30	
		0	1
Pin31	0	x	EP MODE
	1	ROM	EEPROM

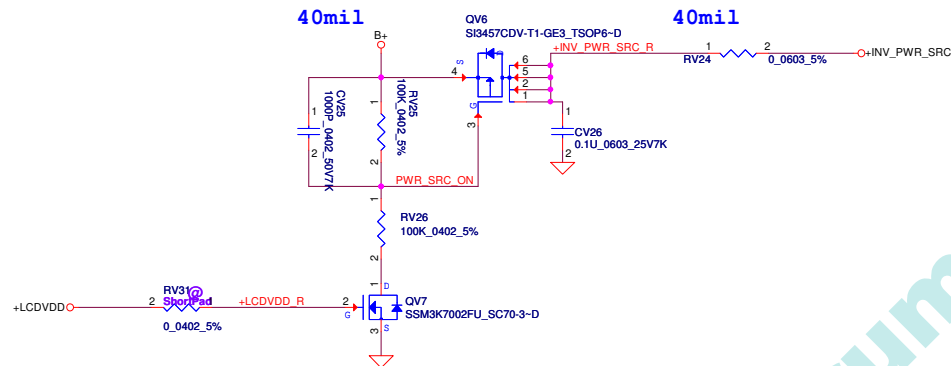


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		Deciphered Date		2014/03/12	
				Document Number	
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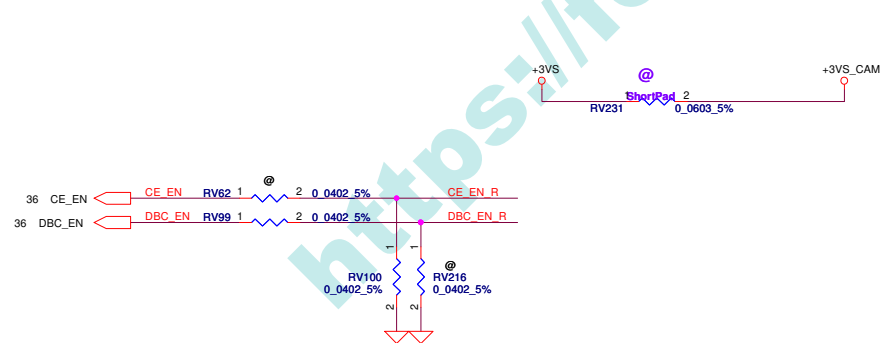
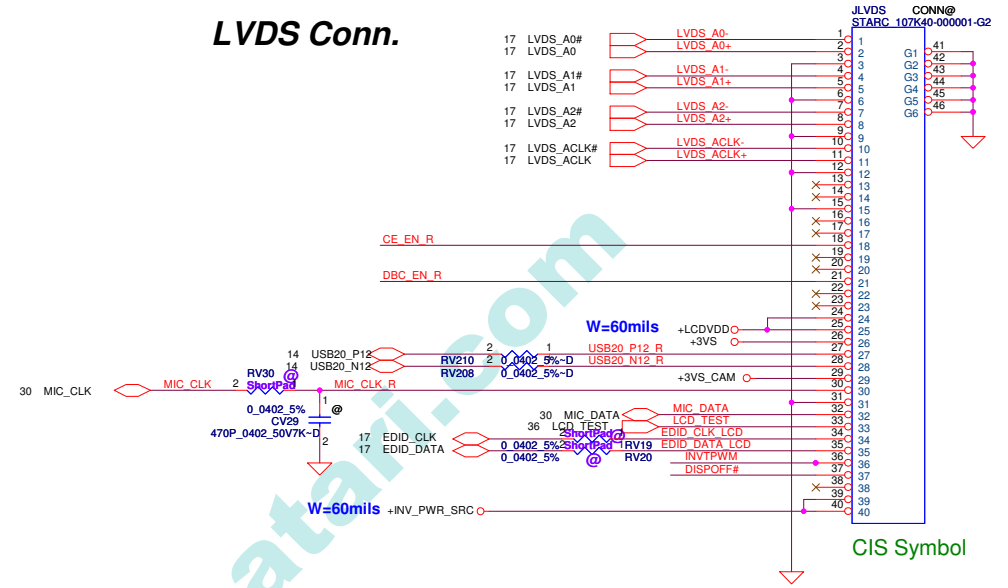
LCD PWR CTRL



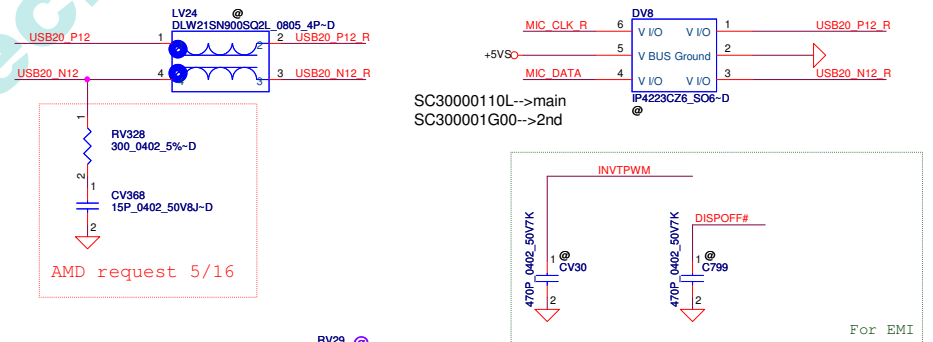
LCD backlight PWR CTRL



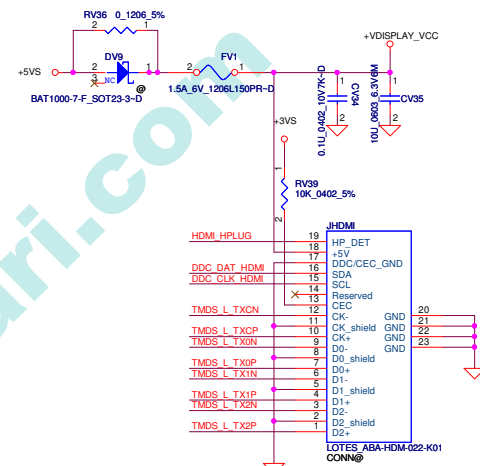
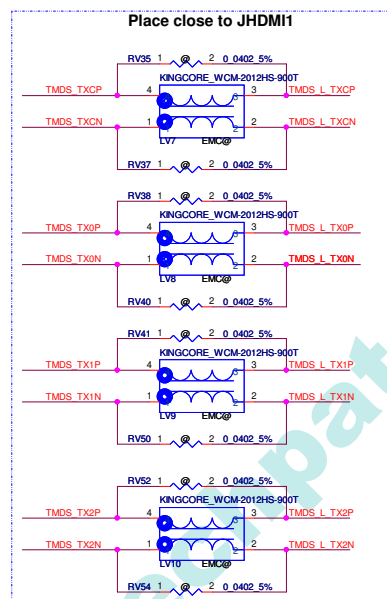
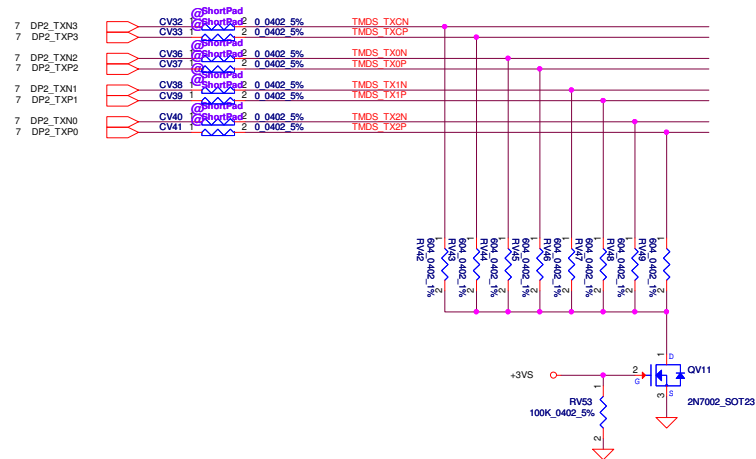
Wedcam PWR CTRL

**LVDS Conn.**

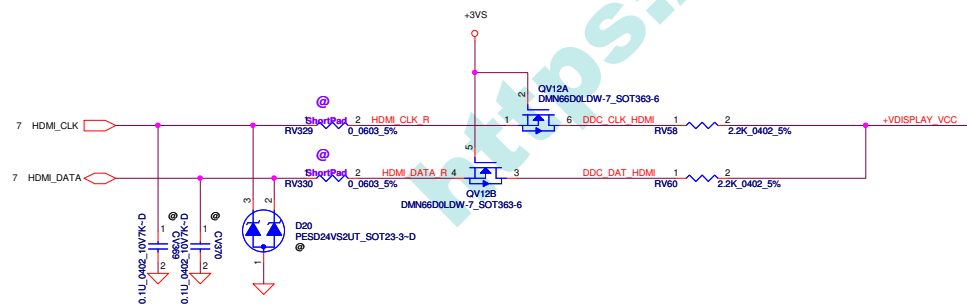
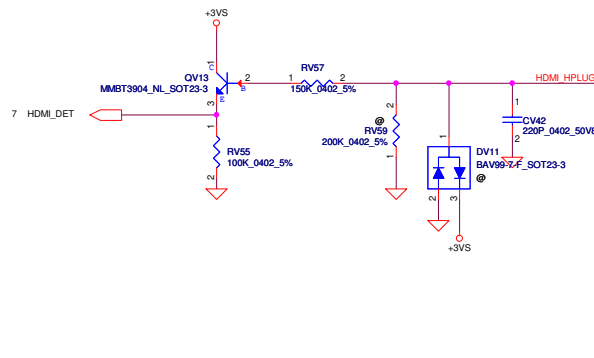
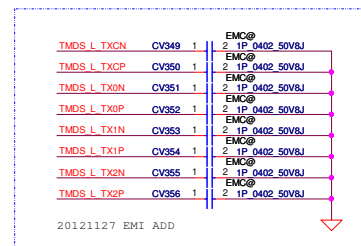
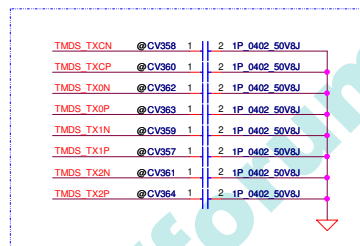
** Reserved for EMI/ESD/RF
need to close to JLVDS*



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Issued Date	2012/09/11	Deciphered Date	2014/03/12	Document Number	LA-9103P
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Date		Tuesday, November 27, 2012		Sheet	18 of 52

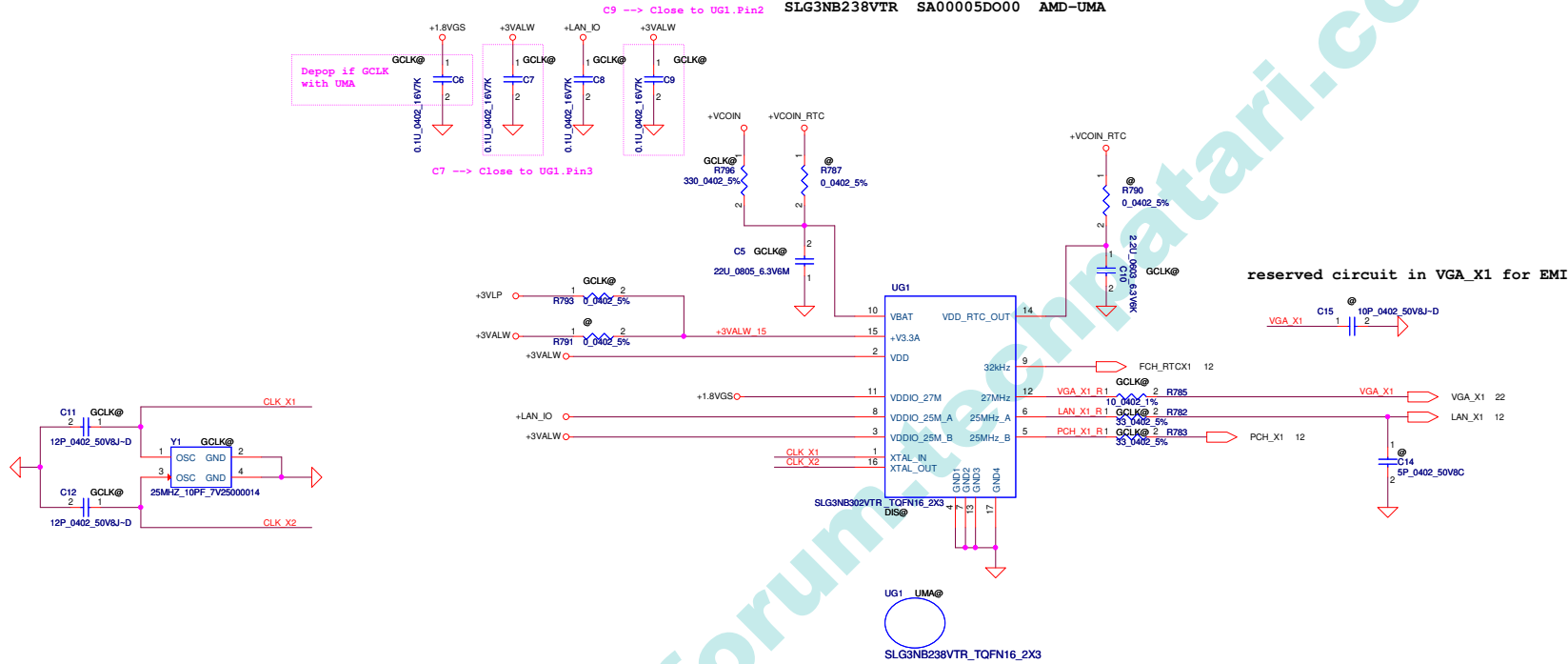


Part Number	Description
R0000000023M	HDMI W/Logo:R0000000023M



CV365, CV367
Please close APU side

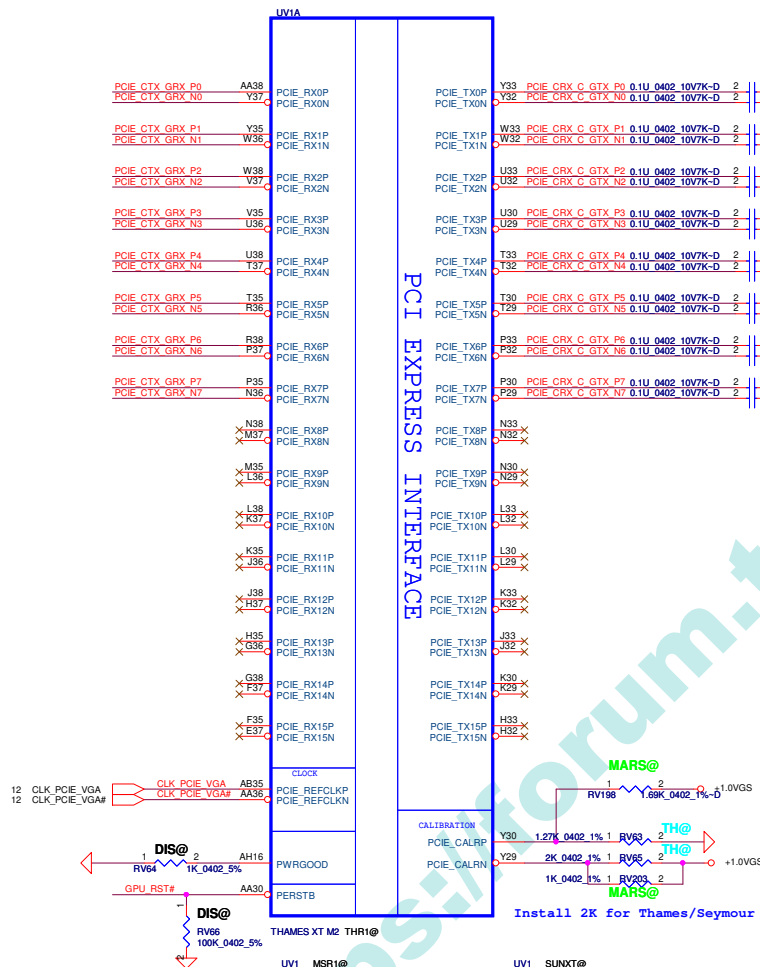
SLG3NB244VTR SA000057I00 Intel-UMA
 SLG3NB300VTR SA00005RS00 Intel-DIS
 SLG3NB302VTR SA00006D500 AMD-DIS
 SLG3NB238VTR SA00005D000 AMD-UMA



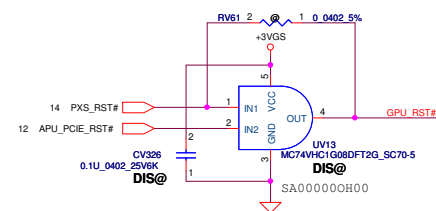
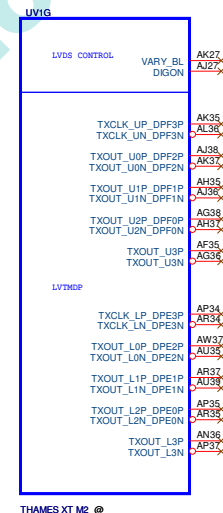
5 PCIE_CTX_GRX_P[7..0] PCIE_CTX_GRX_P[7..0]
5 PCIE_CTX_GRX_N[7..0] PCIE_CTX_GRX_N[7..0]

GFX PCIE LANE REVERSAL

PCIE_CRX_GTX_P[7..0] PCIE_CRX_GTX_P[7..0] 5
PCIE_CRX_GTX_N[7..0] PCIE_CRX_GTX_N[7..0] 5

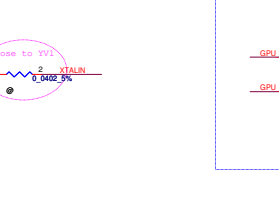
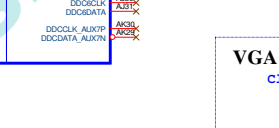
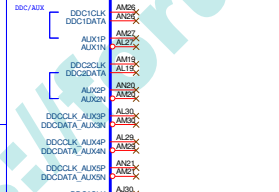
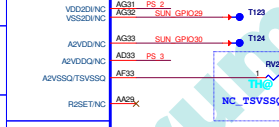
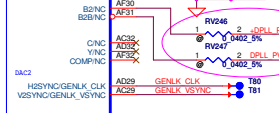
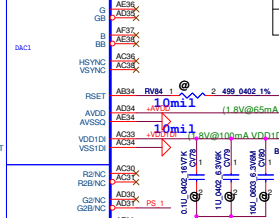
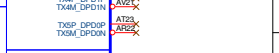
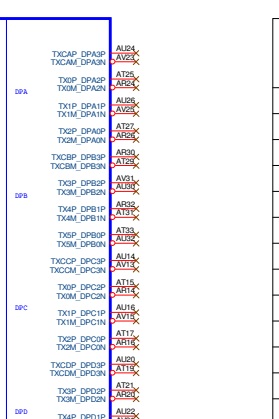
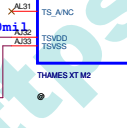
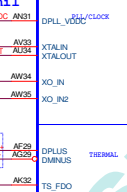
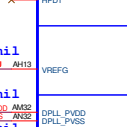
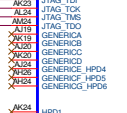
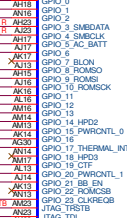
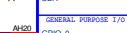
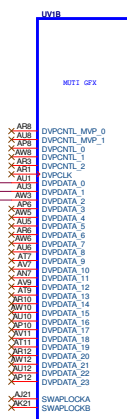
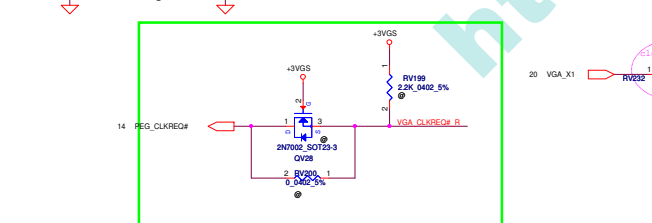
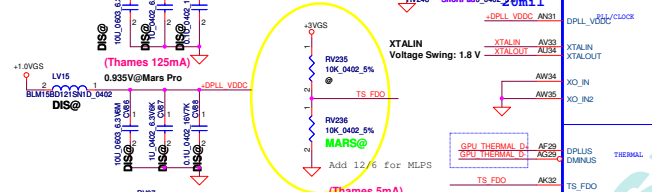
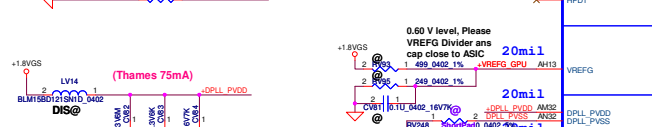
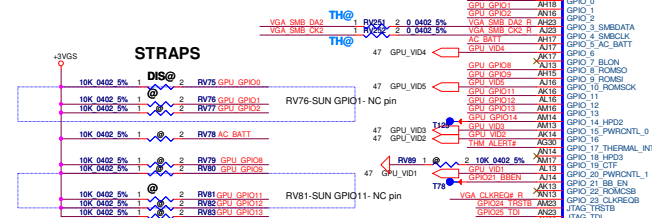


LVDS Interface





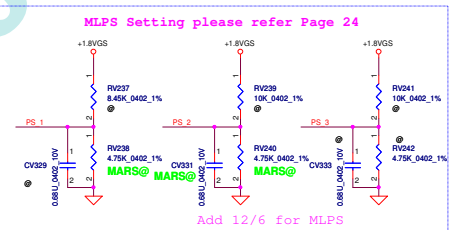
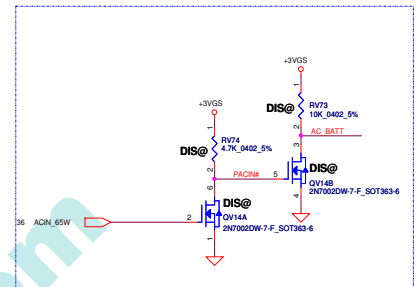
GPI



RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	POE FULL TX OUTPUT SWING 0: 55% swing 1: Full swing	X
TX_DEMPHY_EN	GPIO1	POE TRANSMITTER DE-EMPHASIS 0: disable 1: enable	X
RSVD	GPIO2	Addressed POE speed when compliance test 0: 2.5G/4 1: 5G/4	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_F0MC5B	ENABLED EXTERNAL BIOS ROM 0: disable 1: enable	X
ROMIDCFG(2,0)	GPIO[3:1]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XXX
VP_DEVICE_STRAP_BNA	V2SYNC	IGNORE VP DEVICE STRAPS	0
RSVD	HS2VNC		0
RSVD	GENERICC		0
AUX[1]	HSYNC	AUX[1] AUX[0] 0: 0 No Audio function 0: 1 Audio for DisplayPort and HDMI if dongle is detected	11
AUX[0]	VSYNCR	1: Audio for DisplayPort only 1: Audio for both DisplayPort and HDMI	

GPI021	H2SYNC	GENERICC	GPI02	GPI08
--------	--------	----------	-------	-------



TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)

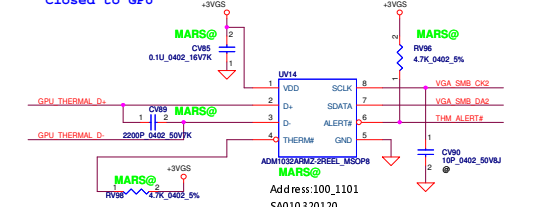
MLPS Bit	AMD recommended setting			
	strap	R_PU	R_PD	C
PS0:	11001	RV243=8.45K	RV201=2K	CV335=NC
PS1:	11000	RV237=NC	RV238=4.75K	CV329=NC
PS2:	00000	RV239=NC	RV240=4.75K	CV331=0.68u

☐ Via call back function:

ID	Memory Type	Configuration	Row x Col x Bank bits	Channel Size
0	Samsung K4W2G1646E-BC11	128Mx16x8pcs	14*10*8	2G(S1G Only)
1	Samsung K4W2G1646E-BC11	128Mx16x8pcs	14*10*8	1G
2	Micron MT41K128M16J-T-107GK	128Mx16x4pcs	14*10*8	1G
3	Hynix H5TC2G63FR-11C	128Mx16x4pcs	14*10*8	1G
4	Samsung K4W4G1646B-HC11	256Mx16x4pcs	15*10*8	2G
5	Micron MT41K256M16HA-107GE	256Mx16x4pcs	15*10*8	2G
6	Hynix H5TC4G63AFR-11C	256Mx16x4pcs	15*10*8	2G
7				

PS_3 CONFIG [2:0]				Memory Configuration					
ID	RV241	RV242	Bits[3:1]	Memory Type	Configuration	Row x Col x Bank bits	Channel Size	VPN	DPN
0	NC	4750	000	Samsung-DDR3	128M x 16 8PCS	14 x 10 x 8	2G	K4W2G1646E-BC11	24880
1	8450	2000	001	Samsung-DDR3	128M x 16 4PCS	14 x 10 x 8	1G	K4W2G1646E-BC11	
2	4530	2000	010	Micron-DDR3	128M x 16 4PCS	14 x 10 x 8	1G	MT41K128M16JT-107G-K	
3	6980	4990	011	Hynix-DDR3	128M x 16 4PCS	14 x 10 x 8	1G	H5TC2G63FFR-11C	
4	4530	4990	100	Samsung-DDR3	256M x 16 4PCS	15 x 10 x 8	2G	K4W4G1646B-HC11	
5	3240	5620	101	Micron-DDR3	256M x 16 4PCS	15 x 10 x 8	2G	MT41K256M16HA-107G-E	
6	3400	10000	110	Hynix-DDR3	256M x 16 4PCS	15 x 10 x 8	2G	H5TC4G63AFR-11C	
7	4750	NC	111						

Closed to GPU

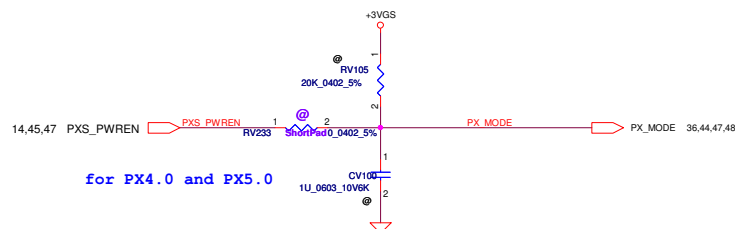


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PX_MODE=1 for Normal Operation
PX_MODE=0 for BACO mode to shut down power rails except VDDR3, PCIE_VDDC and 1.8V rail

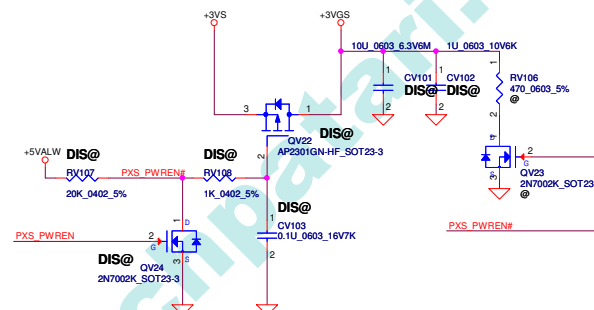
Switch circuits in BACO desings for Thanos/Seymour only

55mA@1.0V, in BACO mode



for PX4.0 and PX5.0

+3.3VS TO +3.3VGS

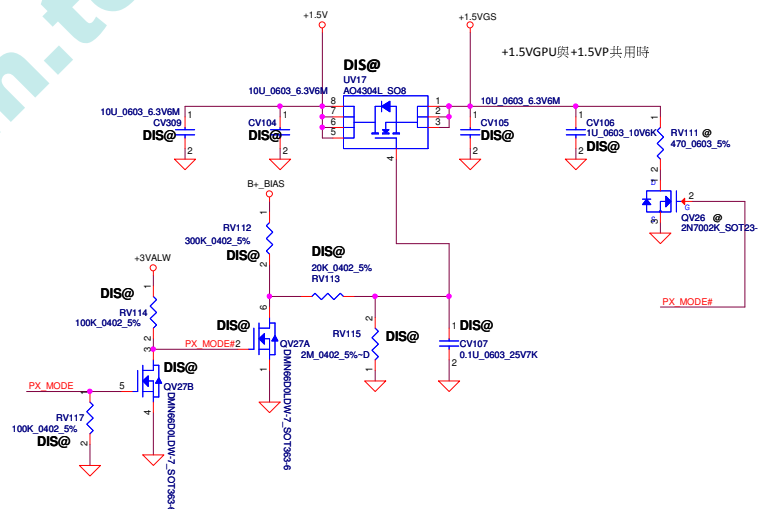


+1.5VGPU TO +1.5VGS



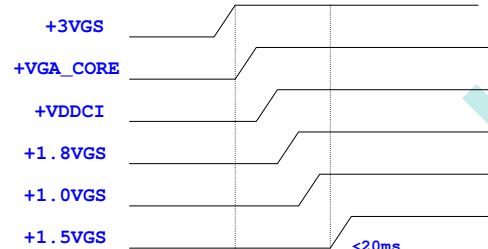
+1.5VGPU直接由Power網路Control

+1.5V TO +1.5VGS

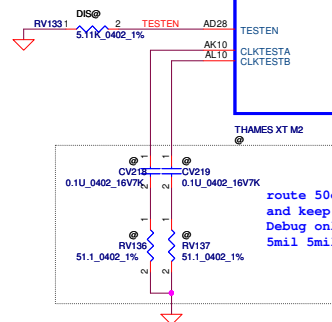
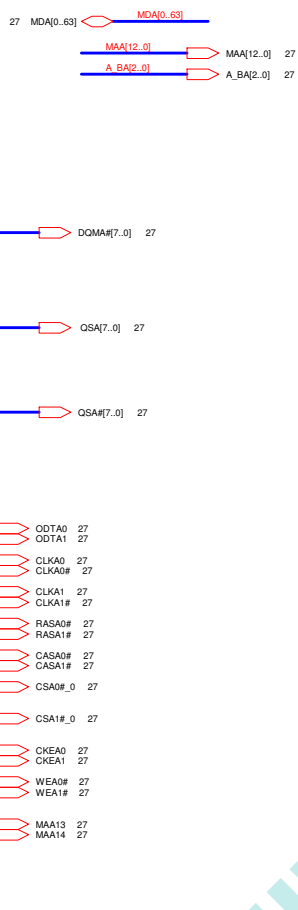


Note:
PX4.0 +VGA_CORE,VDDCI,+1.5VGS OFF
PX4.0 +3VGS, +1.0VGS,+1.8VGS ON
PX5.0 +3VGS,+VGA_CORE,VDDCI,+1.5VGV,+1.0VGS,+1.8VGS OFF

Power Sequence of Thames and Chelsea

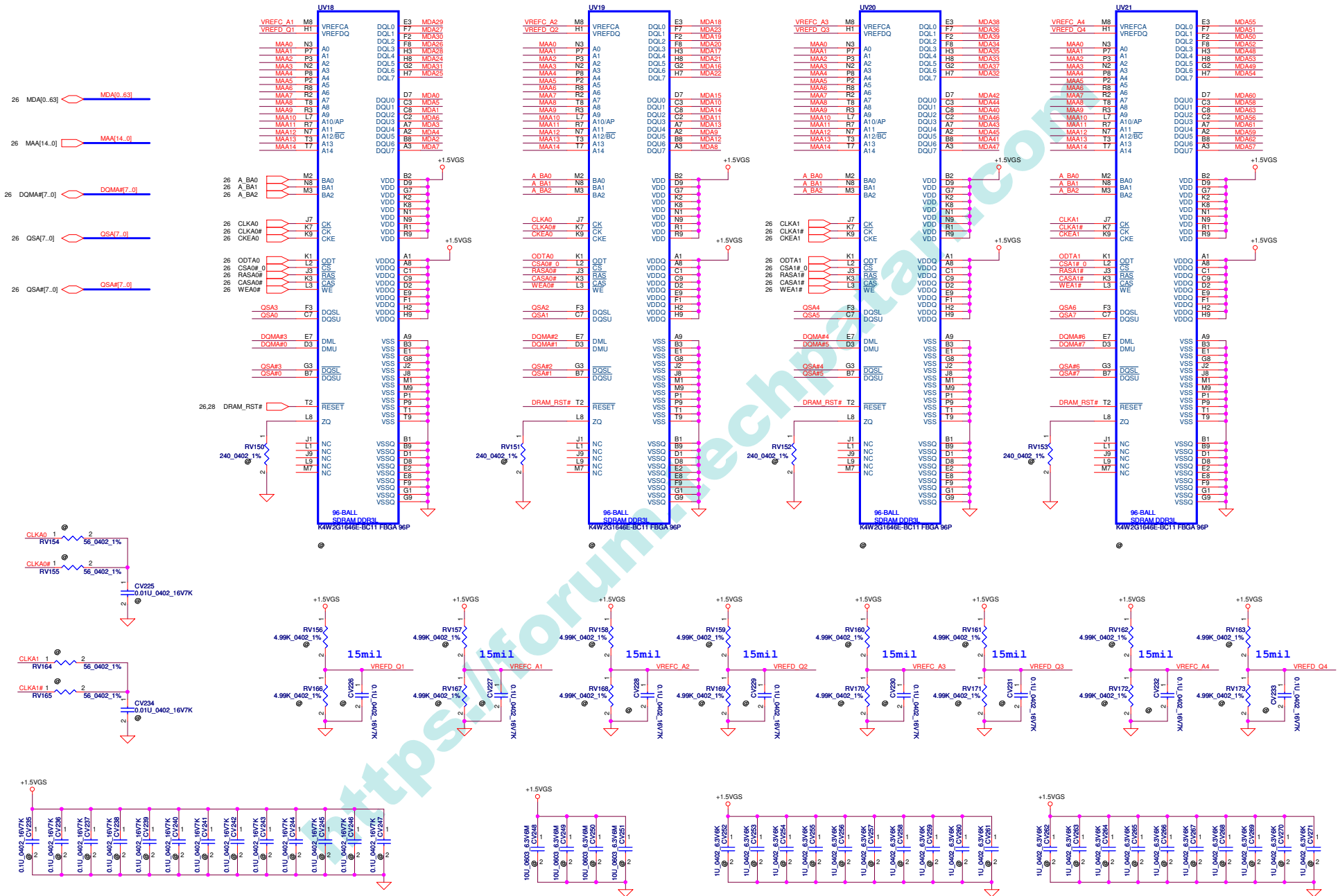


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				Date	Tuesday, November 27, 2012
				Sheet	23 of 52



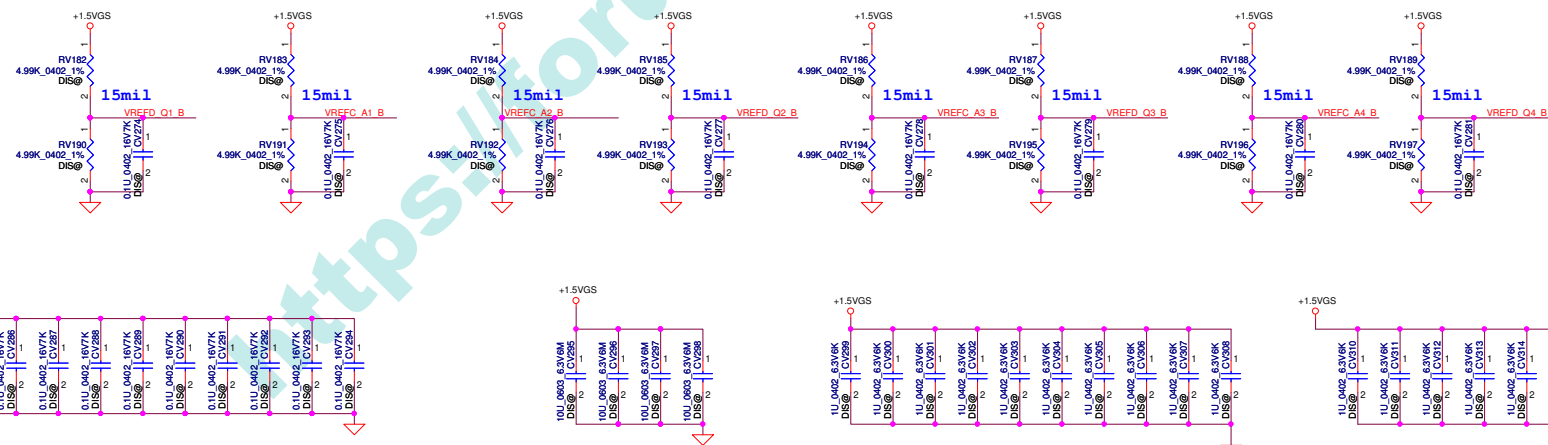
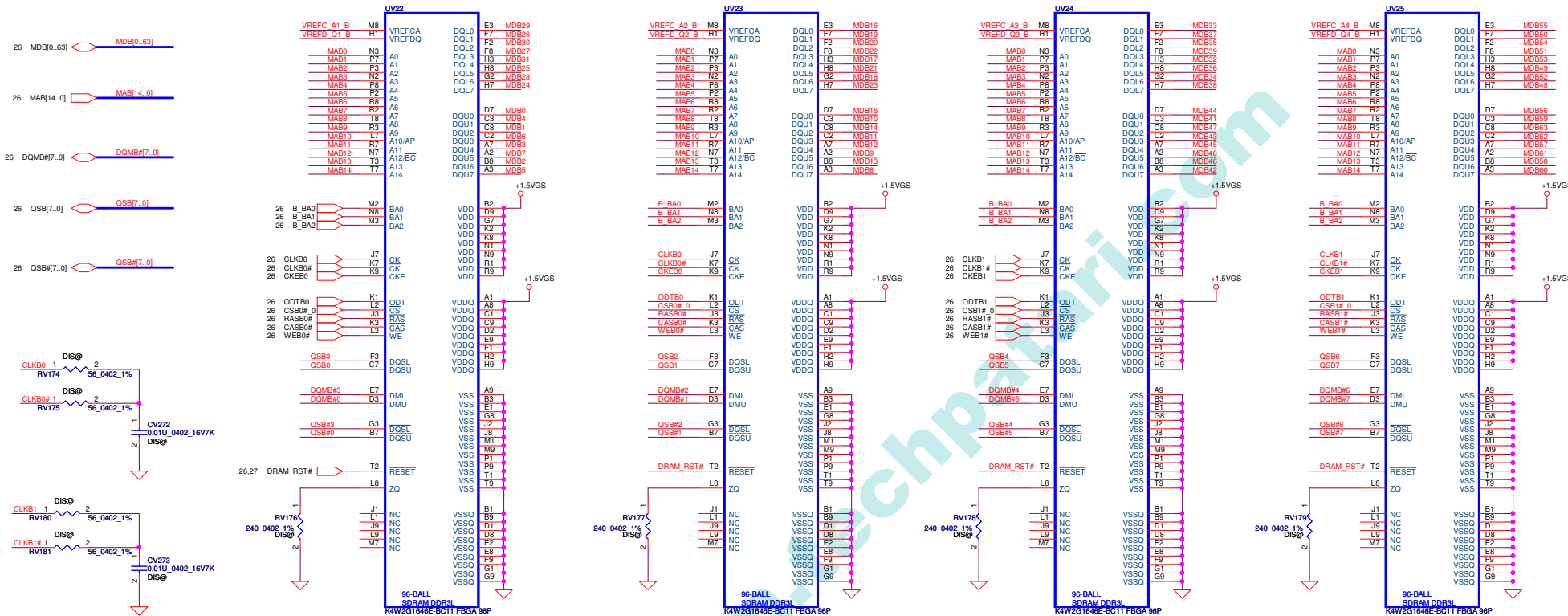
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2012/09/11	Deciphered Date	2014/03/12	Title	ATI ThamesXT M2 MEM IF	
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CHANNEL A: 256MB/512MB DDR3

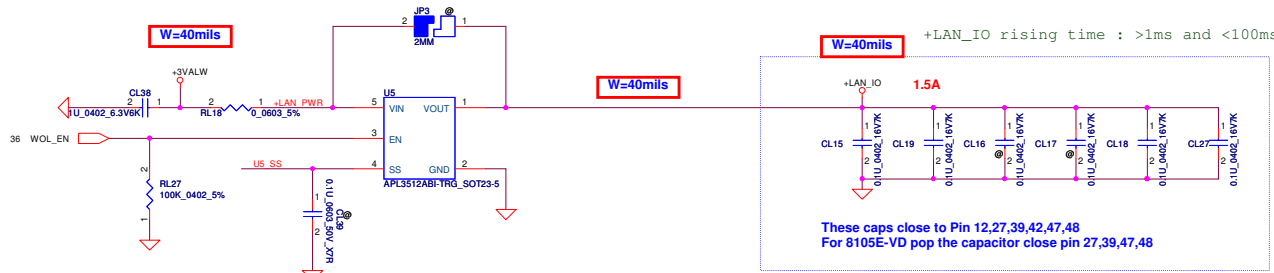


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					LA-9103P	0.1
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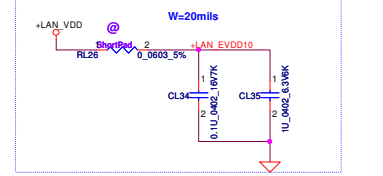
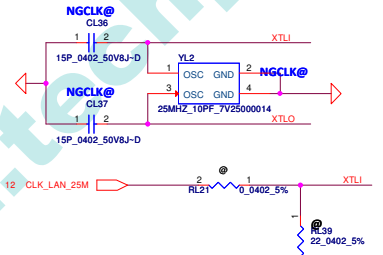
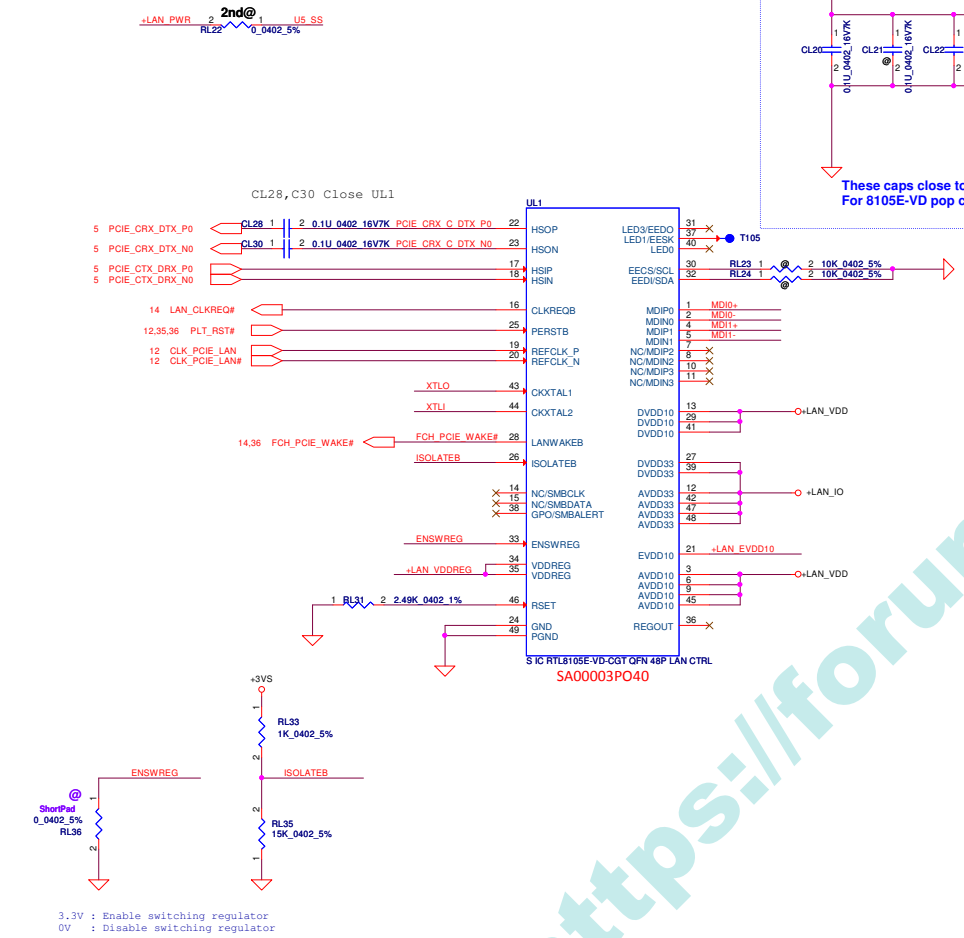
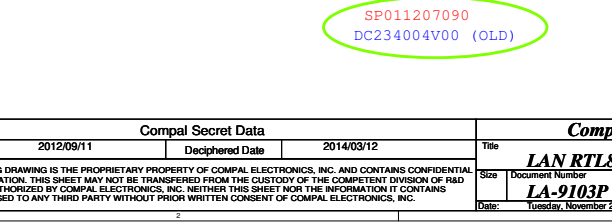
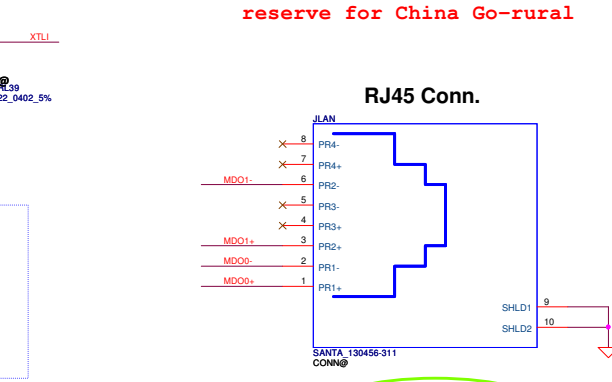
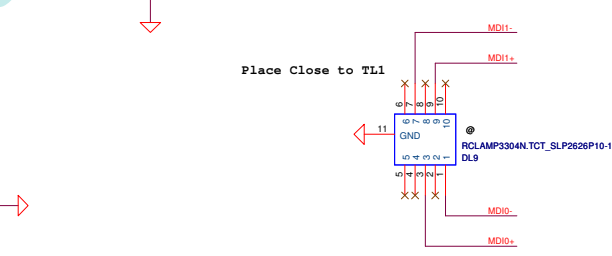
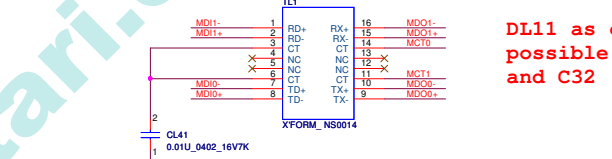
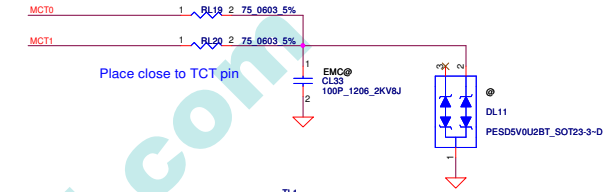
CHANNEL B: 256MB/512MB DDR3



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reserve for China Go-rural

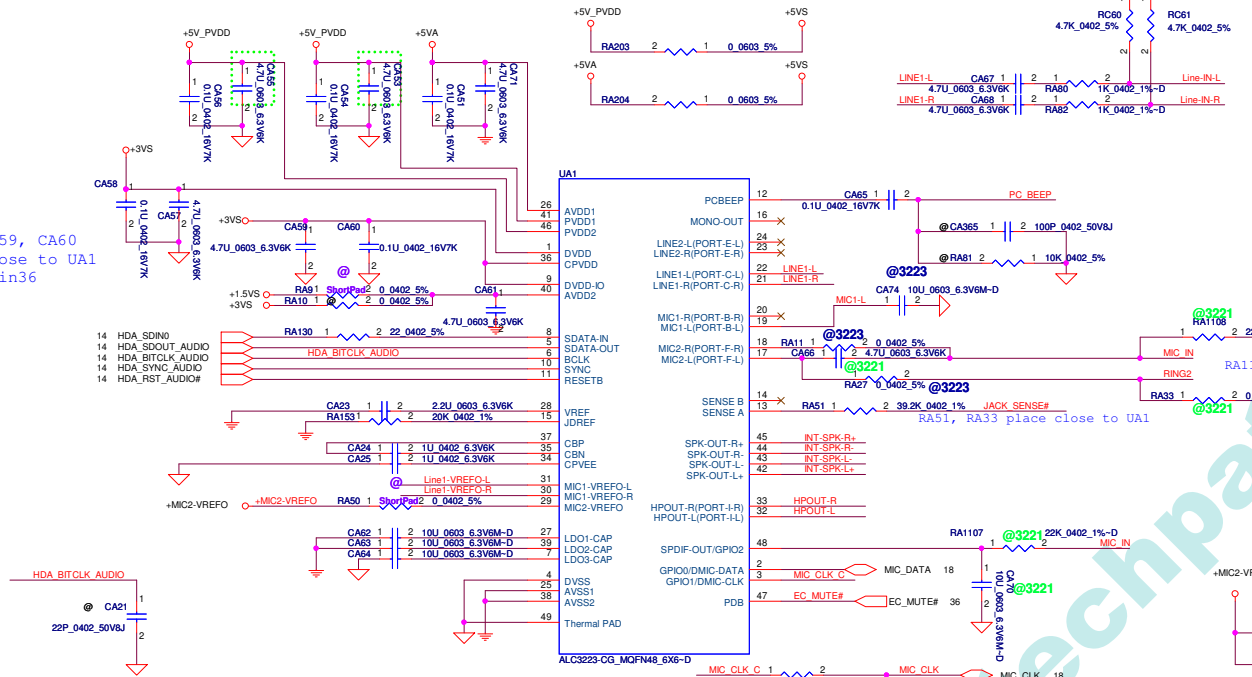


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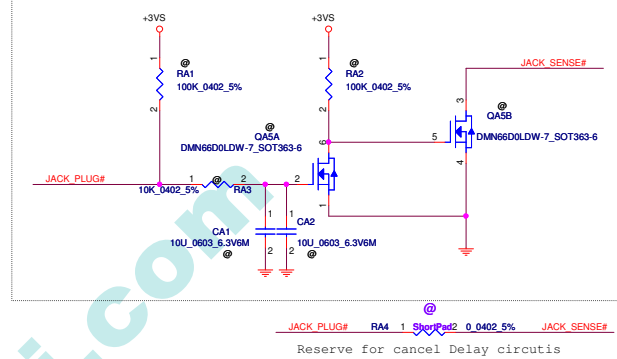


CA71, CA51 place close to Pin 26

CA59, CA60
Close to UA1
Pin36

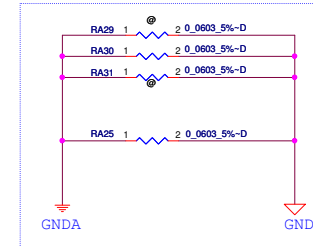


JACK_PLUG Delay circuitis

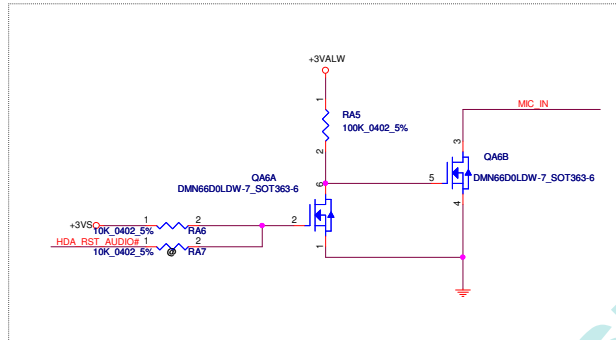
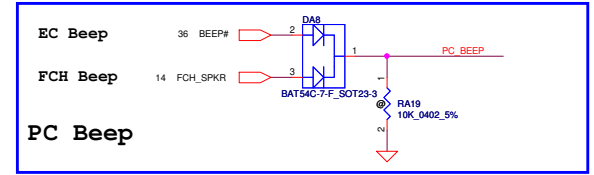


JACK_PLUG# R A1 1 0.0402 5% JACK_SENSE#

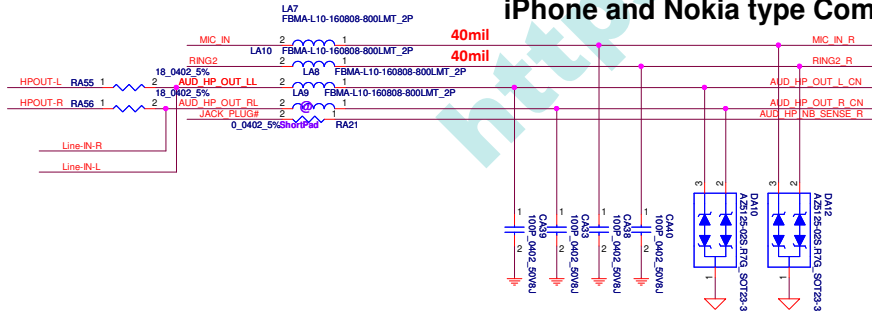
Reserve for cancel Delay circuitis



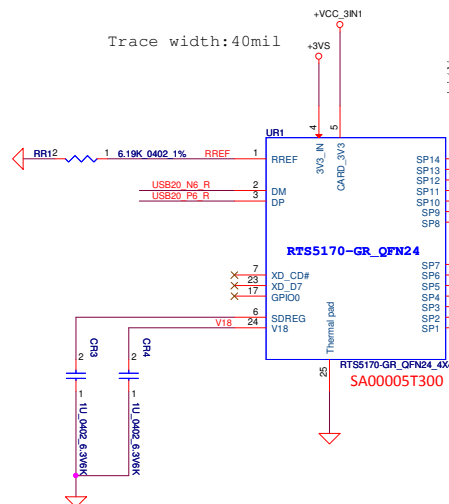
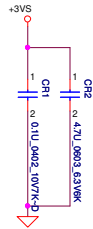
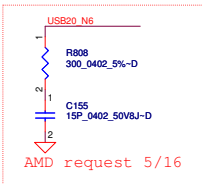
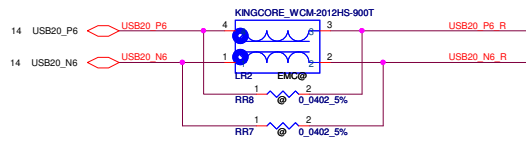
Place on the moat between GND & GNDA.



iPhone and Nokia type Combo Jack

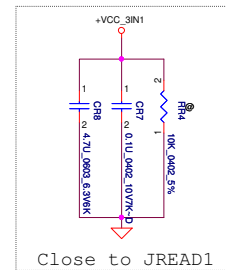
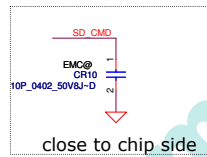
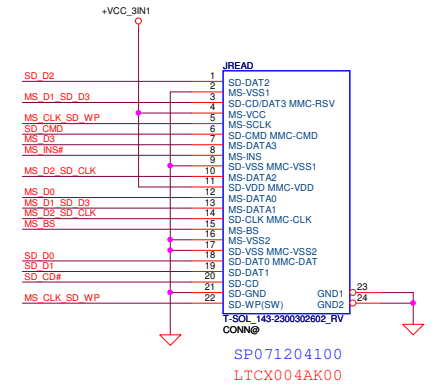
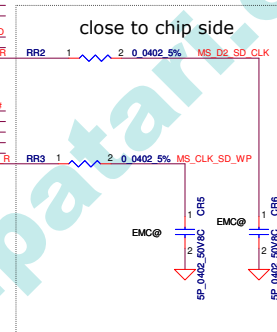


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					Audio Codec ALC3221
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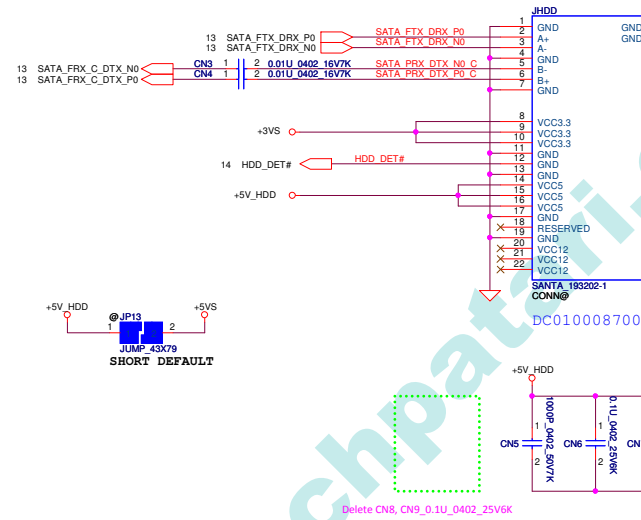
拉MS_D2_SD_CLK到Conn pin 14 SD_CLK
再打Via拉到pin 10 MS_D2

拉MS_CLK_SD_WP到Conn pin 5 MS_CLK
再打Via拉到pin 22 SD_W



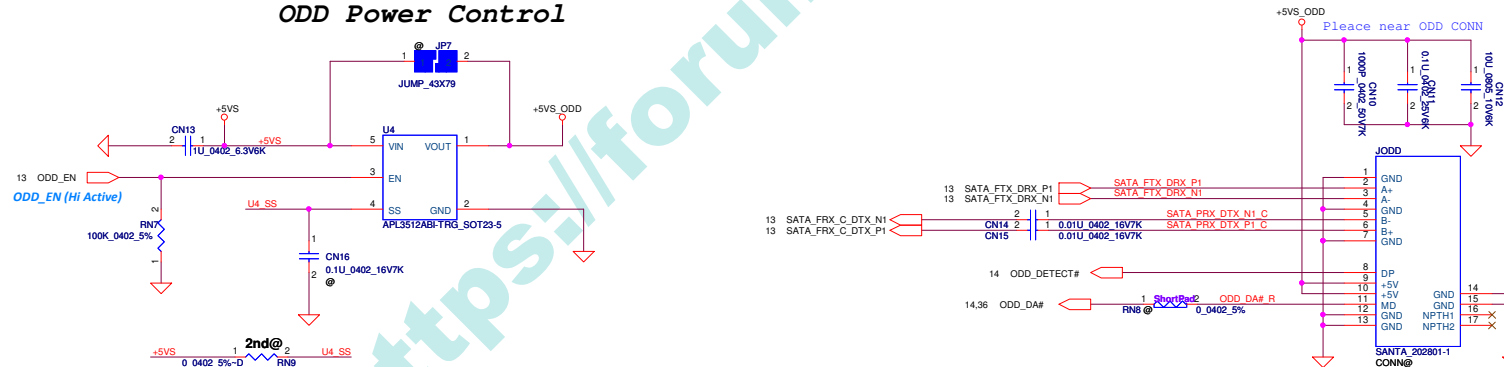
SATA HDD Conn.

+5V_HDD Source

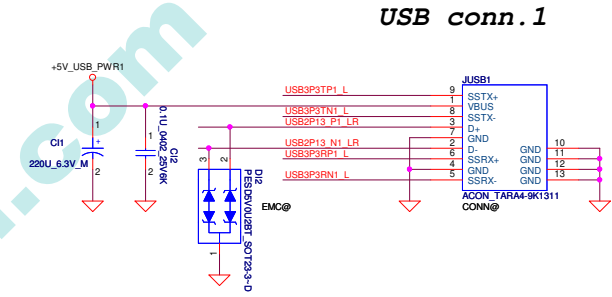
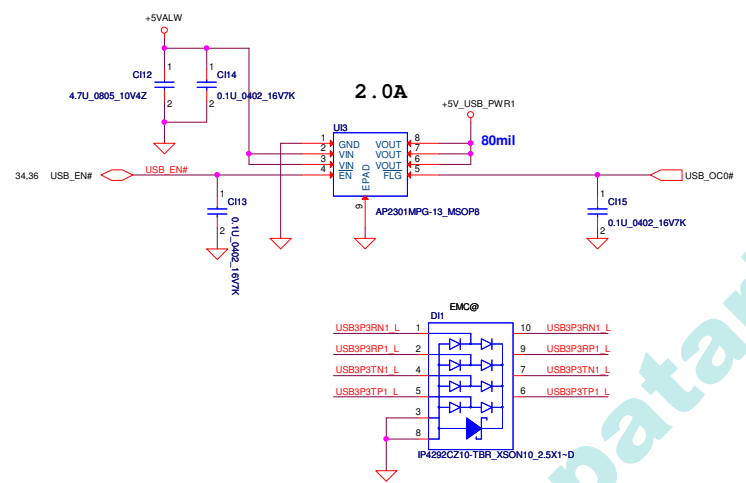
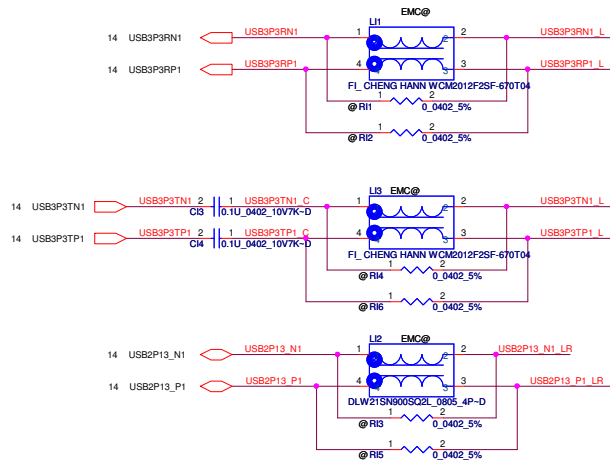


SATA ODD Conn.

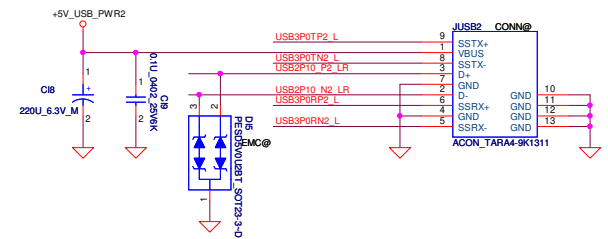
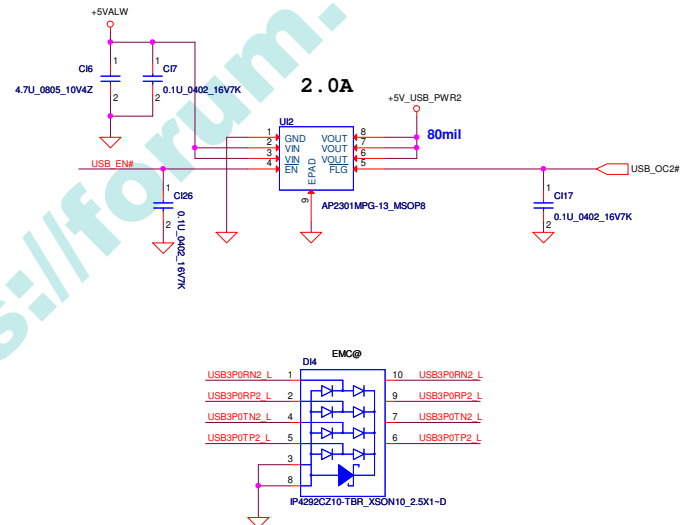
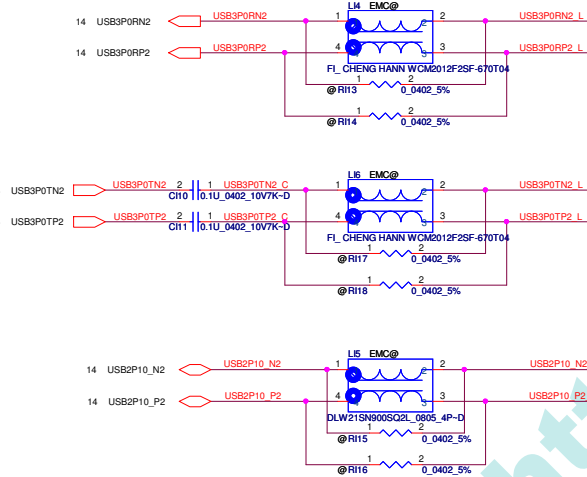
ODD Power Control



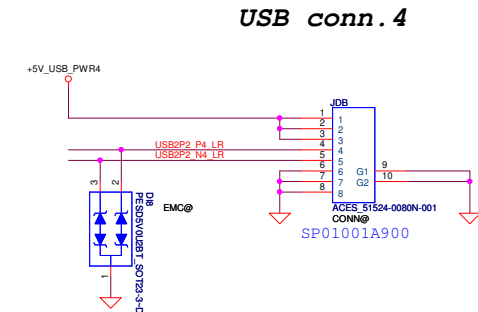
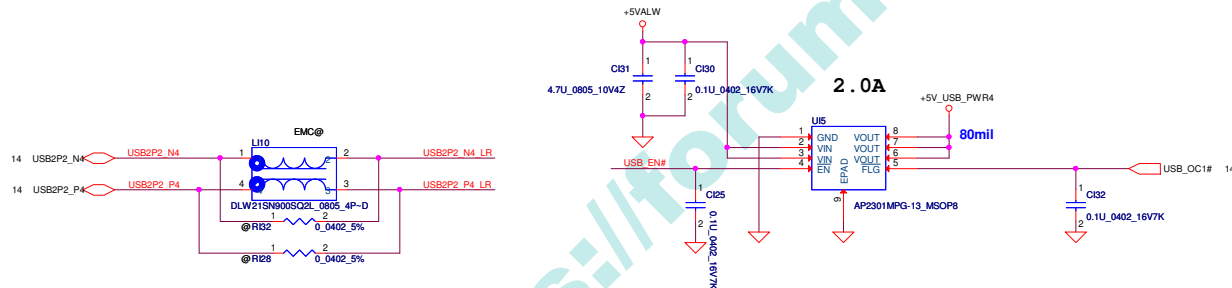
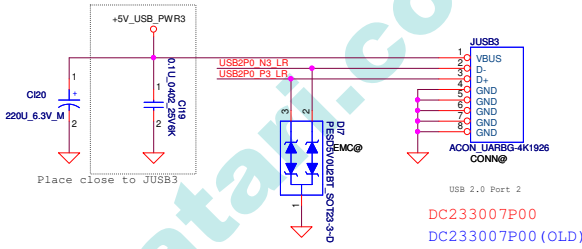
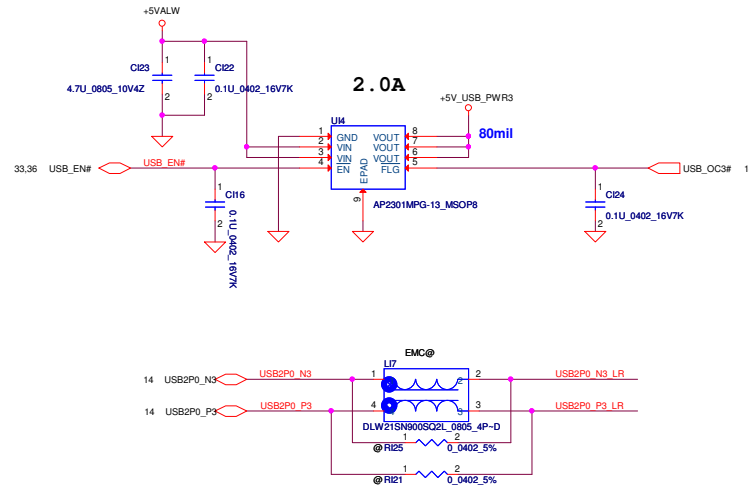
9/20 OAK Intel USB3.0 issue
 Change LI1, LI3, LI4, LI6 Part
 PN: from SM01002080L (S SUPPRE_ MURATA DLW21SN900SQ2L 0805)
 To SM070000580 (S COM FL_ CHENG HANN WCM2012F2SF-670T04)



USB conn.1

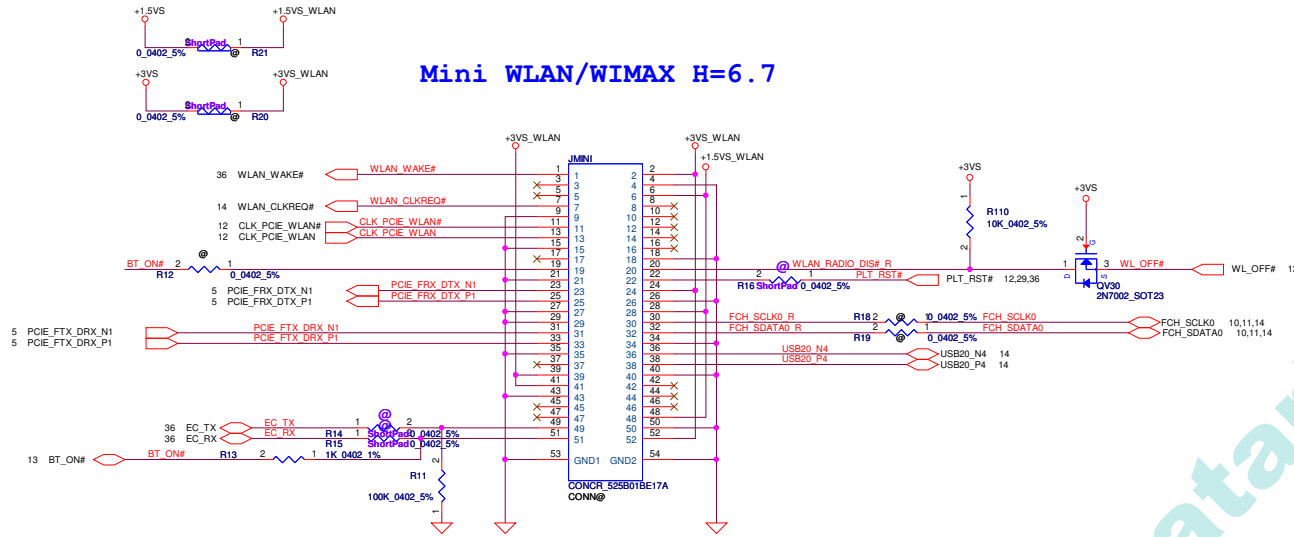


USB conn.2

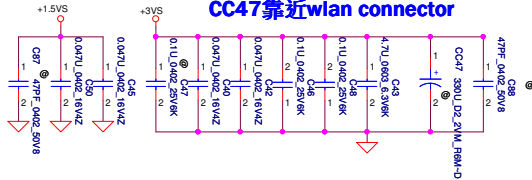


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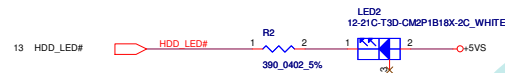
Mini WLAN/WIMAX H=6.7



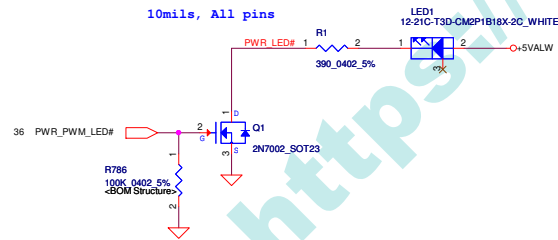
CC47靠近wlan connector



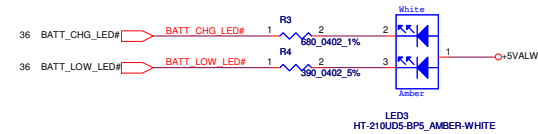
HDD LED



Power LED



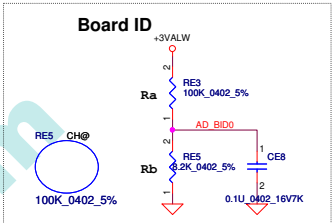
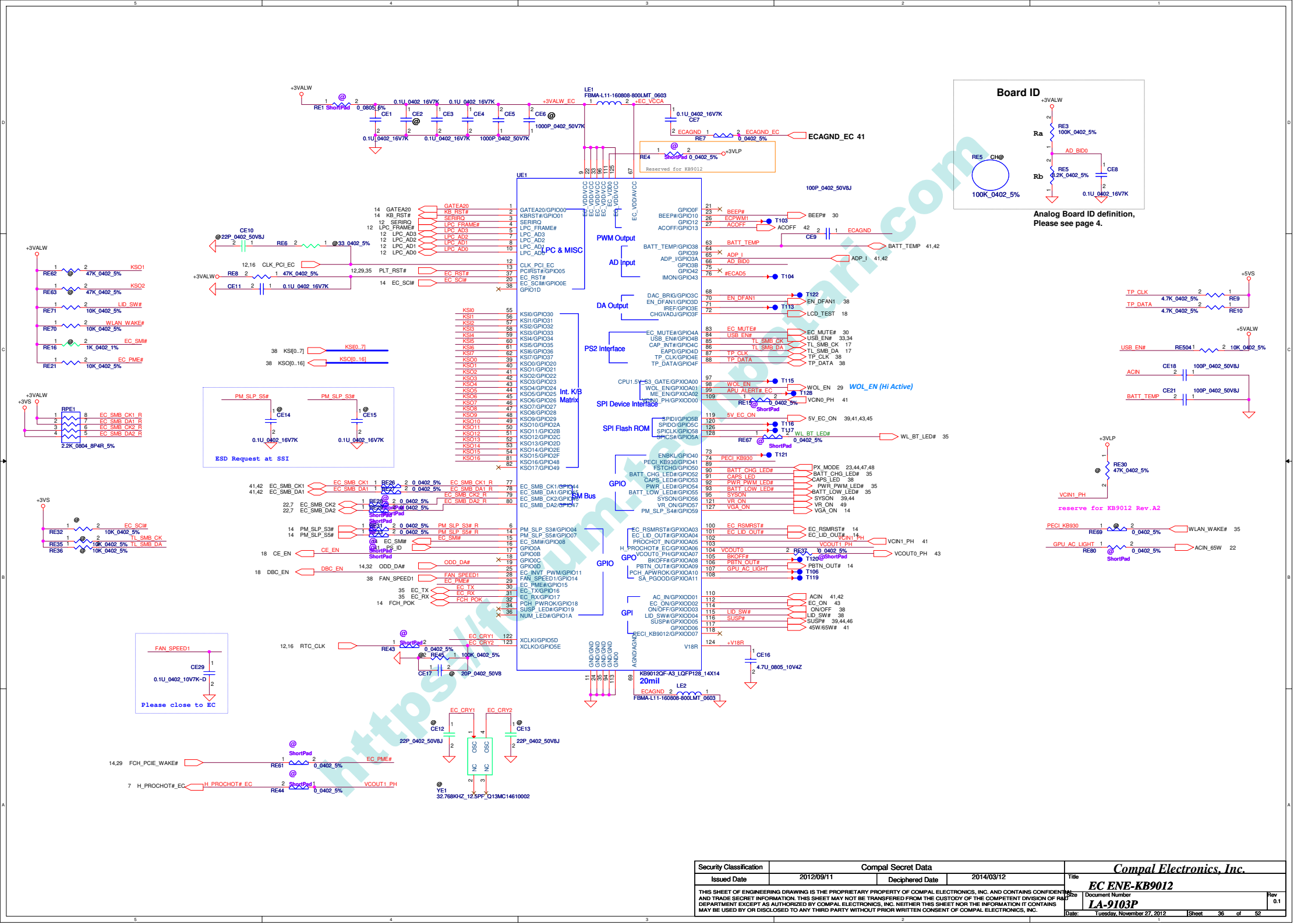
Battery LED



Wireless LED



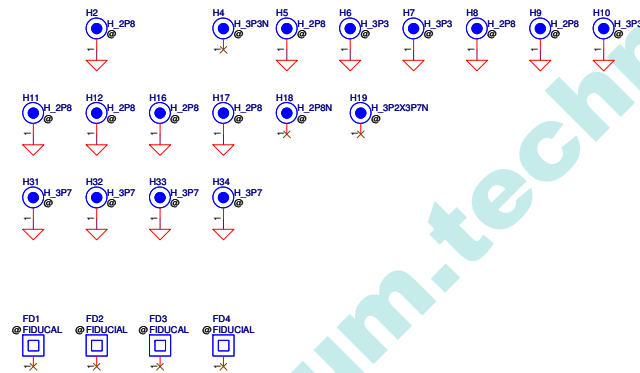
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/09/11	Deciphered Date	2014/03/12	Title	Mini Card/LED
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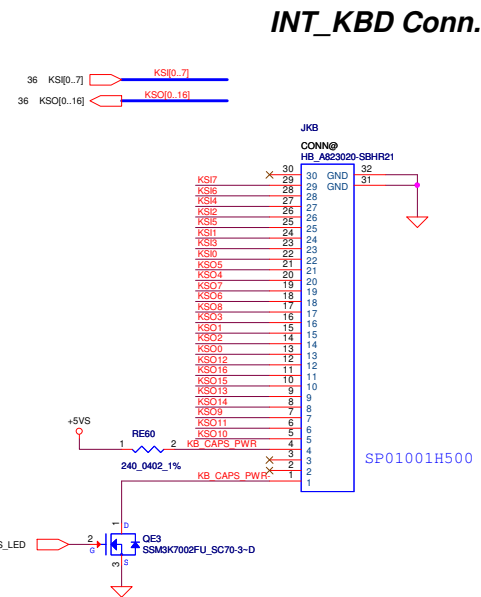
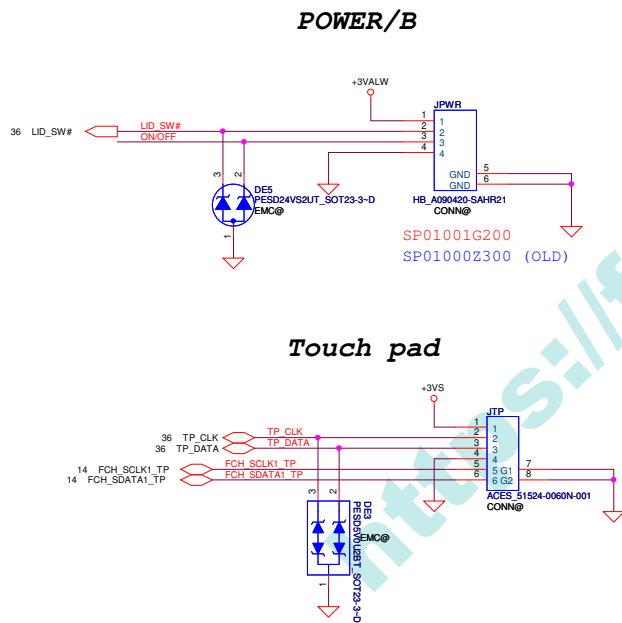
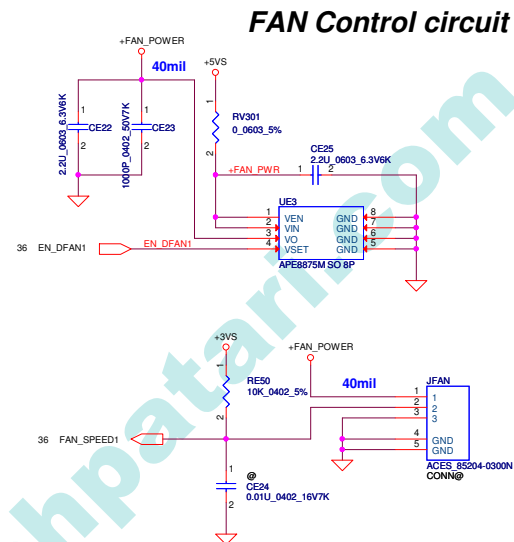
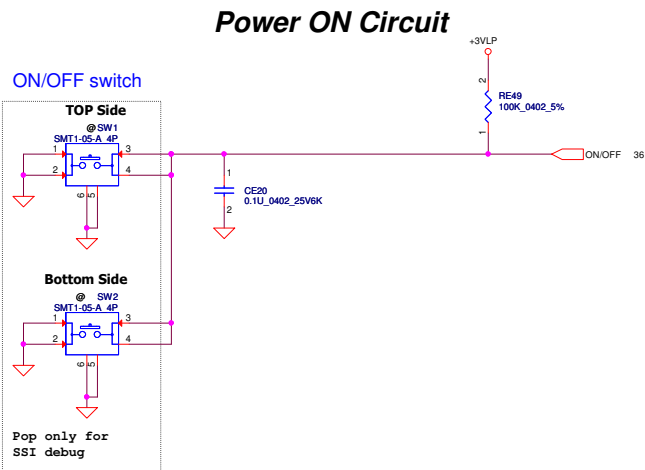
Analog Board ID definition, Please see page 4.

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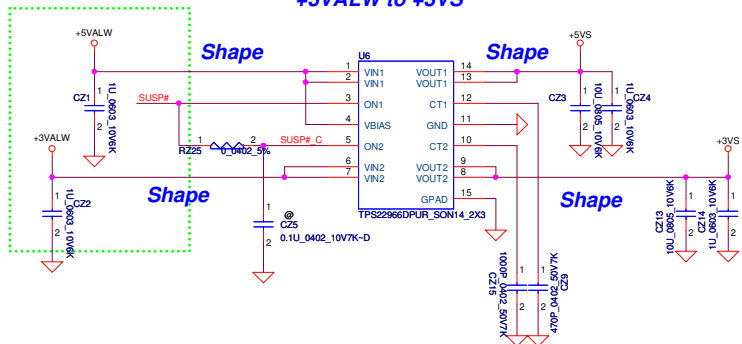
Screw Hole



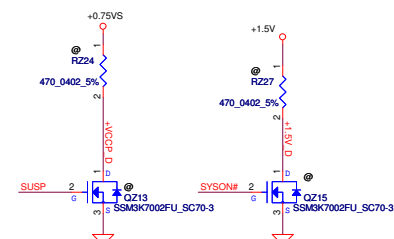
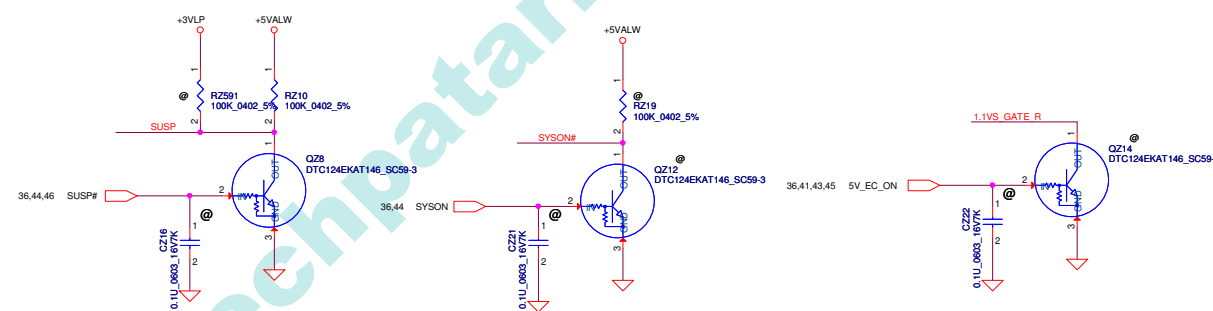
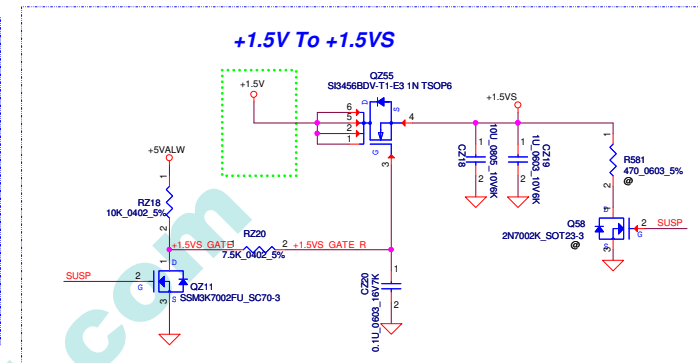
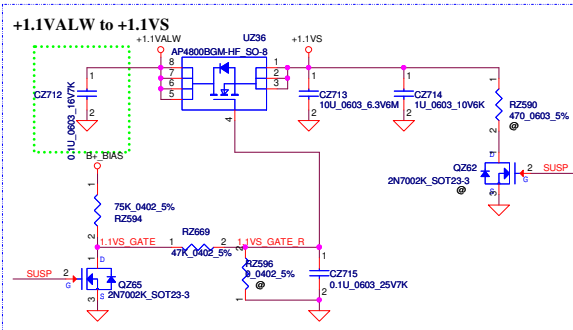
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Issued Date	2012/09/11	Deciphered Date	2014/03/12	Title	Screw Hole
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+5VALW to +5VS
+3VALW to +3VS



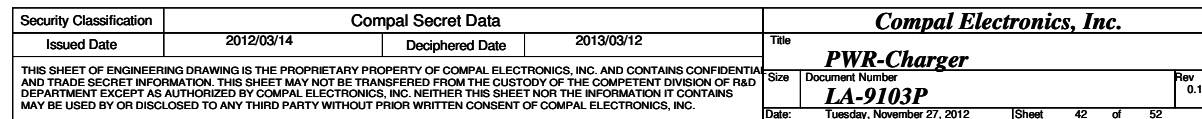
CTx (pF)	RISE TIME (µs)	
	5V	3.3V
0	124	88
220	481	323
470	855	603
1000	1724	1185
2200	3328	2240
4700	7459	4950
10000	16059	10835



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3.3VALWP
TDC 5.4A
Peak Current 7.7A
OCP current 9.2A
TYP MAX
H/S Rds (on) : 23.2mohm , 27.8mohm
L/S Rds (on) : 11.5mohm , 14mohm

5VALWP
TDC 5.6A
Peak Current 8A
OCP current 9.6A
TYP MAX
H/S Rds (on) : 23.2mohm , 27.8mohm
L/S Rds (on) : 11.5mohm , 14mohm

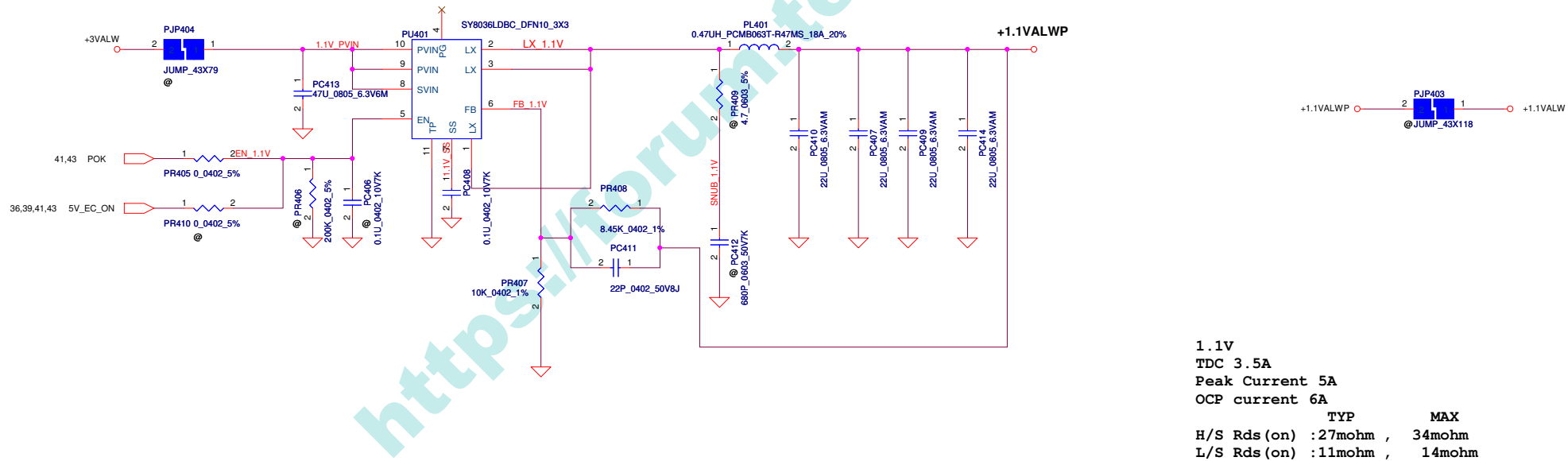
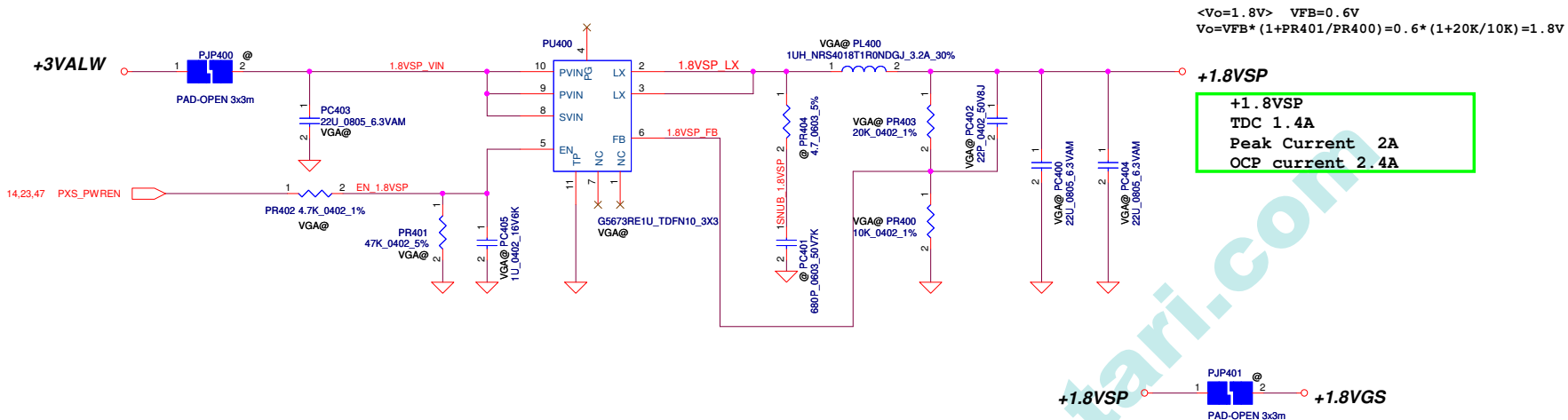
1.5VP
TDC 11A
Peak Current 16A
OCP current 19A

	TYP	MAX
H/S Rds (on)	: 23.2mohm	, 27.8mohm
L/S Rds (on)	: 7mohm	, 8.4mohm

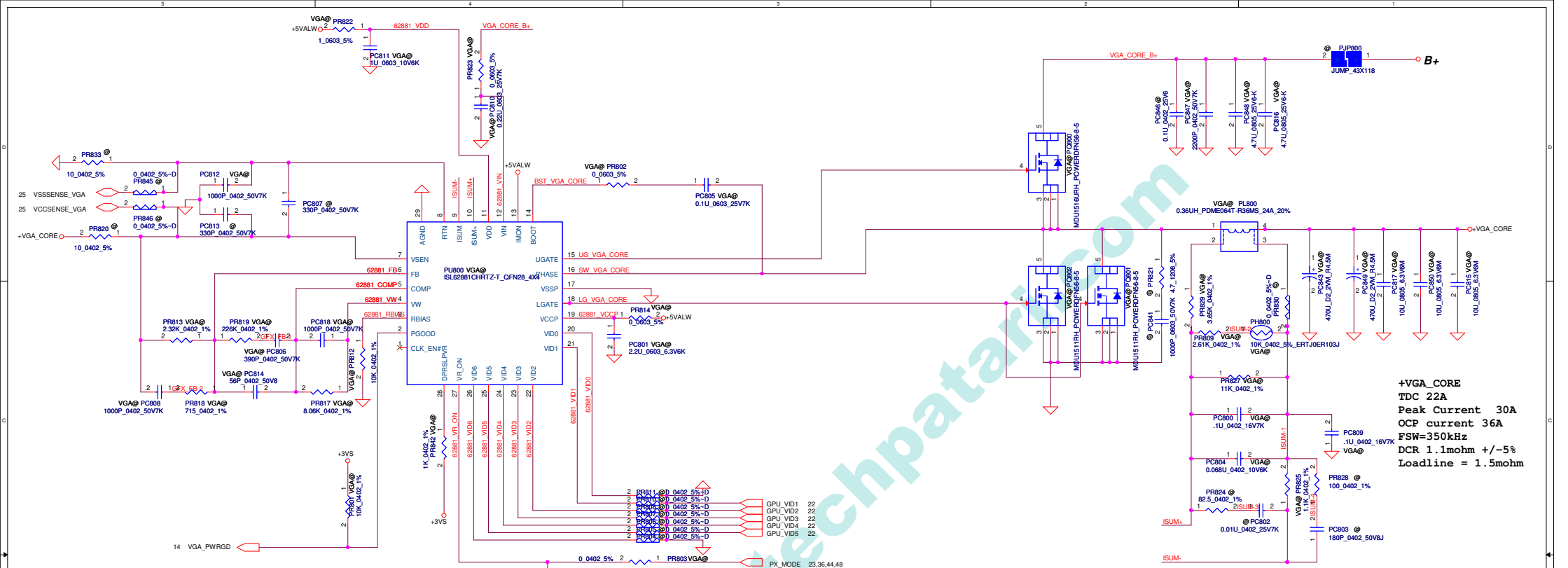
0.75VSP
TDC 0.7A
Peak Current 1A
OCP Current 1.2A

+1.5VGPU
TDC 5.6A
Peak Current 8A
OCP current 9.6A

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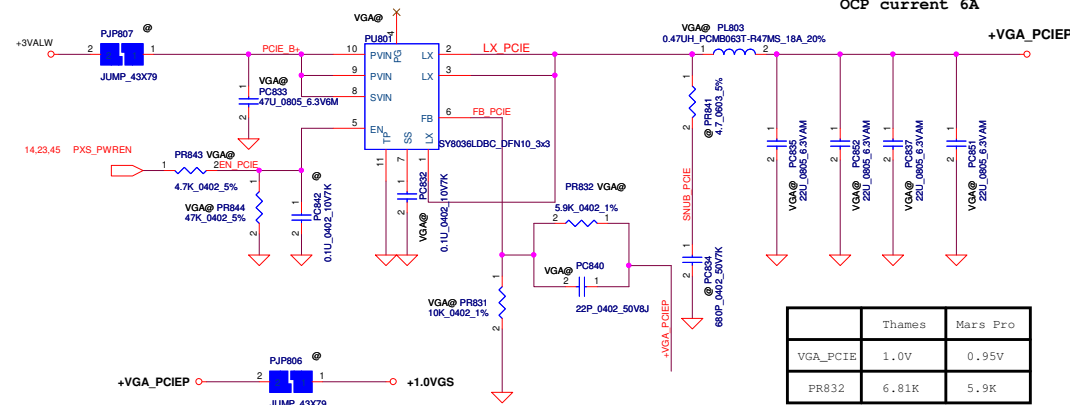
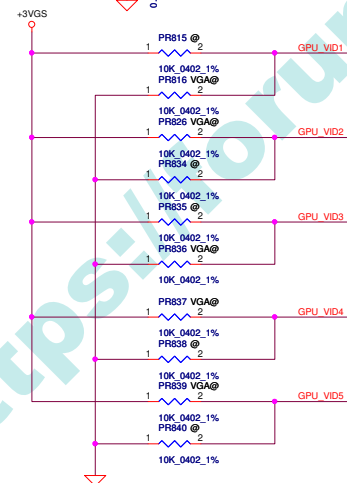


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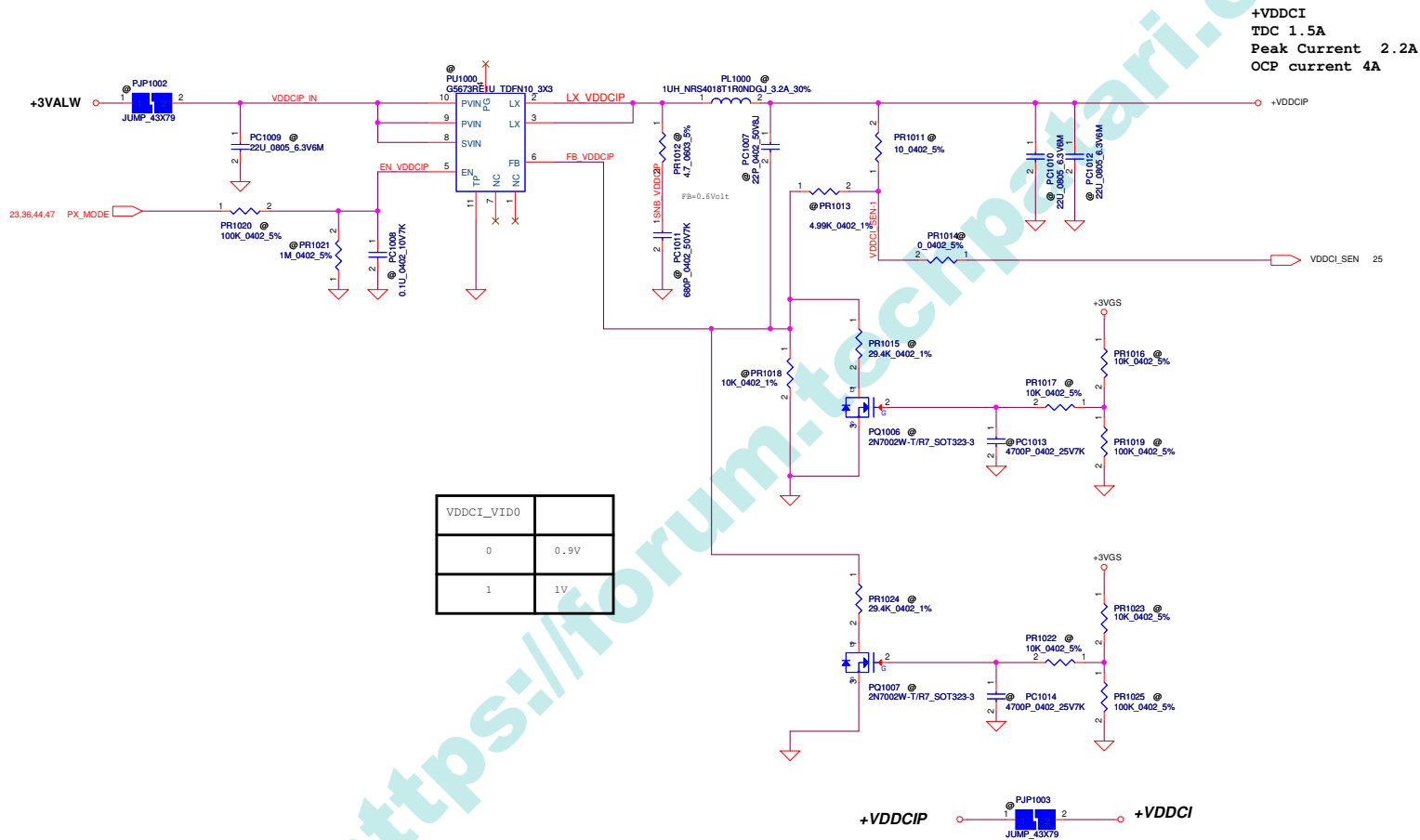


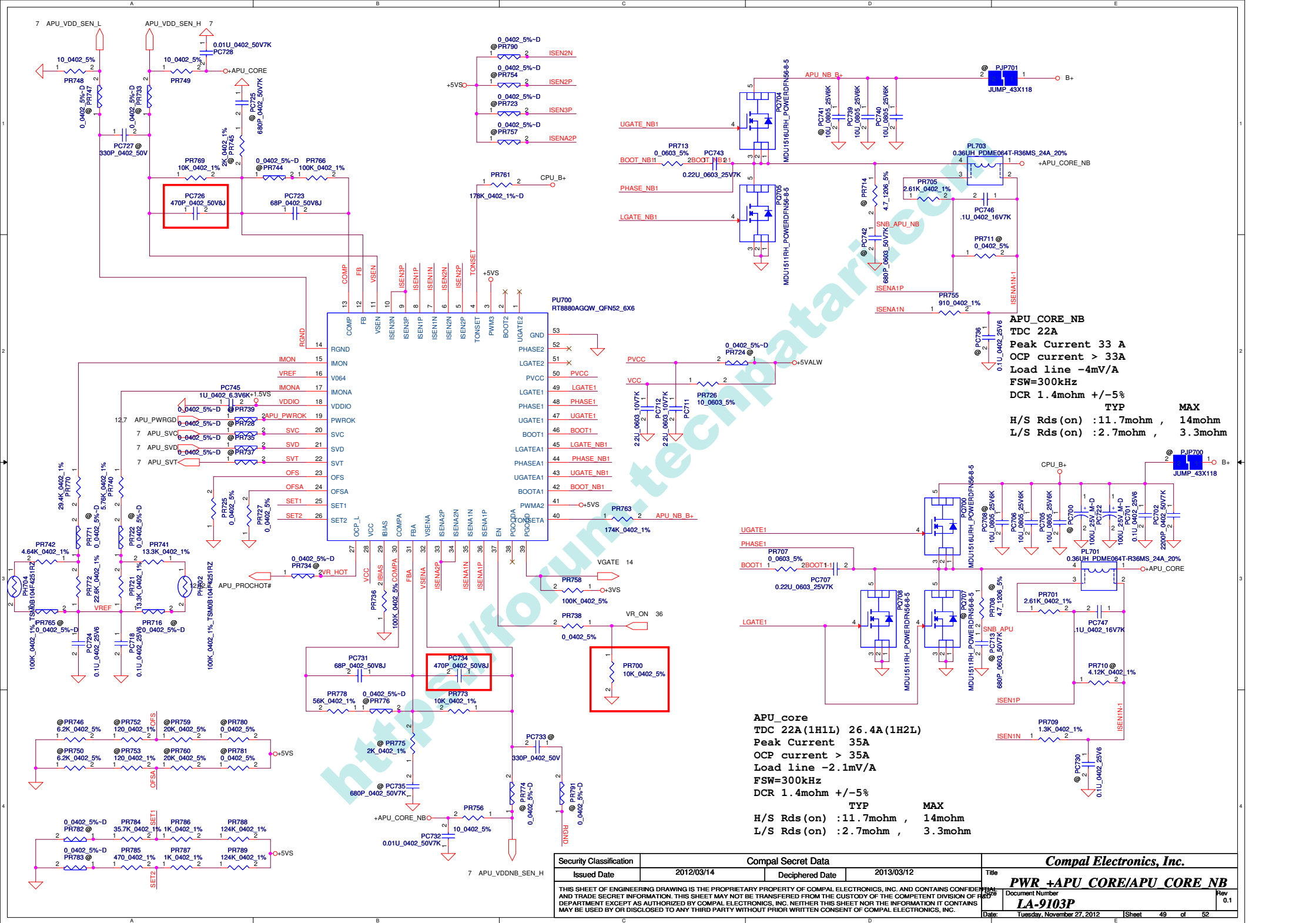
Mars Pro

GPU_VID5 (GPIO_10)	GPU_VID4 (GPIO_14)	GPU_VID3 (GPIO_15)	GPU_VID2 (GPIO_16)	GPU_VID1 (GPIO_20)	Core Voltage Level
0	1	1	1	1	1.125V
1	0	0	0	0	1.1V
1	0	0	0	1	1.075V
1	0	0	1	0	1.05V
1	0	0	1	1	1.025V
1	0	1	0	0	1V
1	0	1	0	1	0.975V
1	0	1	1	0	0.95V
1	0	1	1	1	0.925V
1	1	0	0	0	0.9V
1	1	0	0	1	0.875V
1	1	0	1	0	0.85V
1	1	0	1	1	0.825V
1	1	1	0	0	0.8V
1	1	1	0	1	0.775V



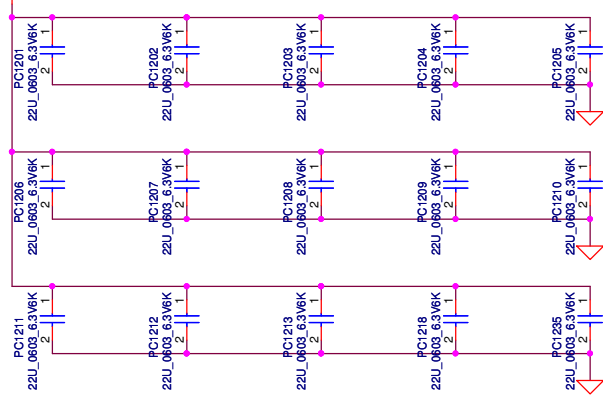
	Thames	Mars Pro
VGA_PCIE	1.0V	0.95V
PR832	6.81K	5.9K



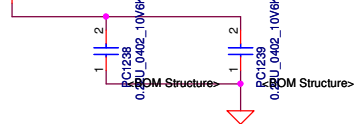


+APU_CORE

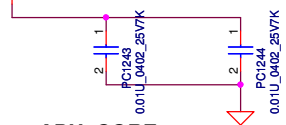
+APU_CORE



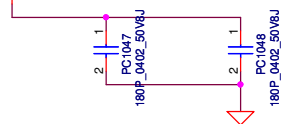
+APU_CORE



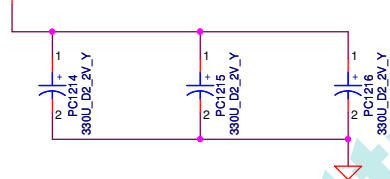
+APU_CORE



+APU_CORE

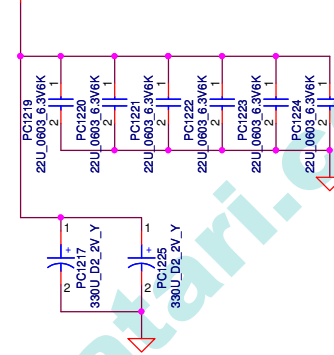


+APU_CORE



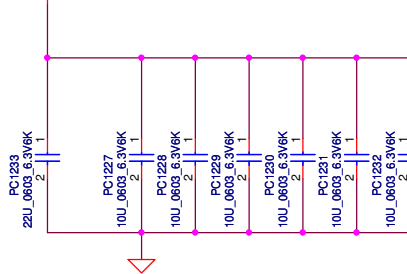
+APU_CORE_NB

+APU_CORE_NB



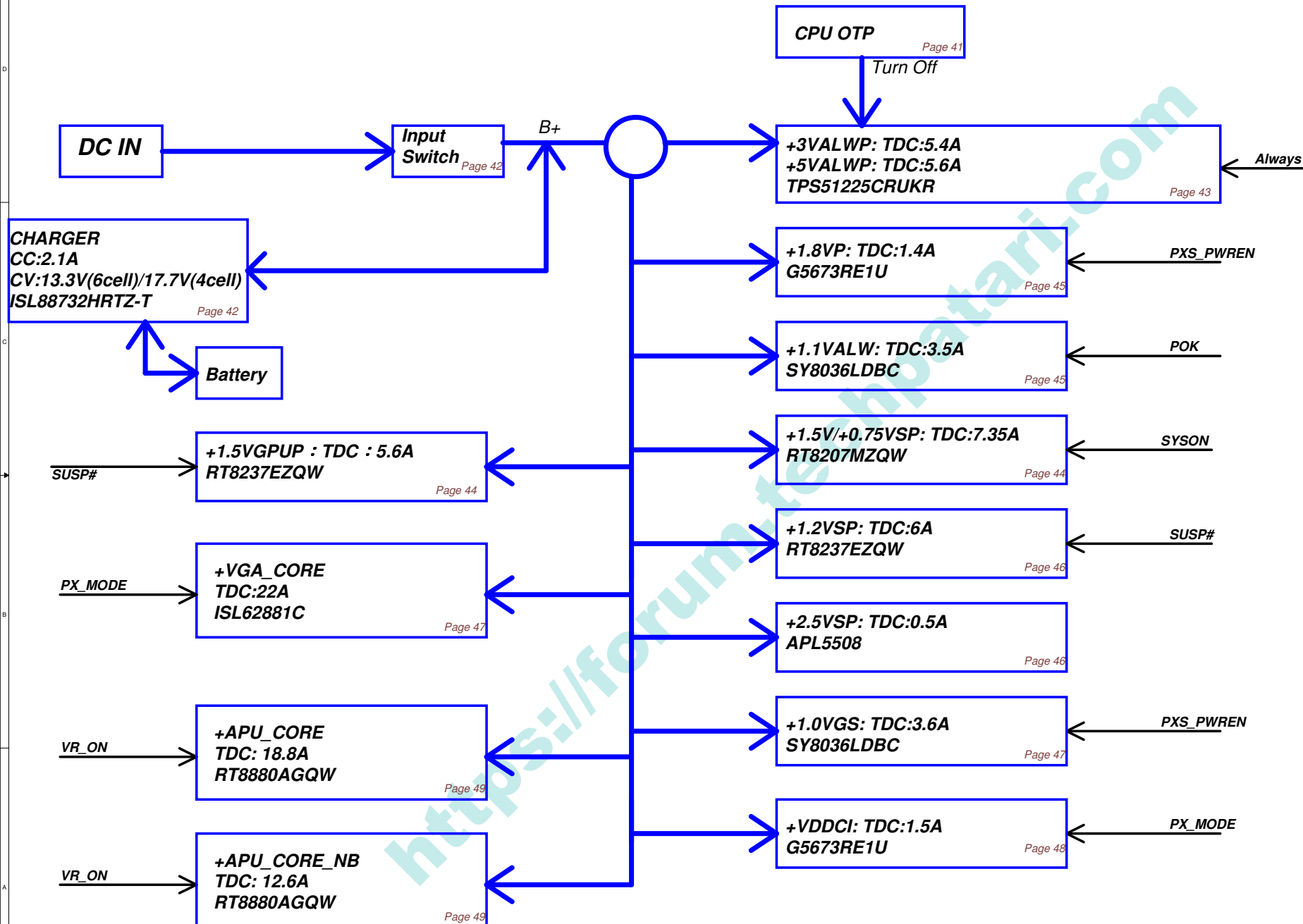
+1.2VS

+1.2VS



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Power block



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